Resistor networks and transfer resistance matrices

W. R. B. Lionheart, K. Paridis, ¹ A Adler ²

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¹School of Mathematics, University of Manchester, U.K.

²Systems and Computer Engineering, Carleton University, Canada

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- R is the complete EIT data.

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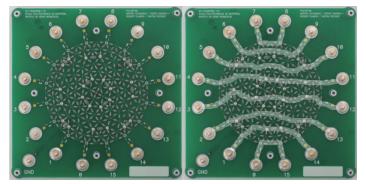
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- It is important to understand the transfer resistance matrices of resistor networks.
- For planar networks this is completely understood, for non-planar less so.

Well connected planar networks

Consider a planar network which can be drawn in a circle with the electrodes ordered anti-clockwise 1,...,L on the circle. Let ${\bf A}$ be the transfer conductance. We will consider only networks that are *well connected*. This means that there are independent paths connecting electrodes in any two non-interleaved subsets of electrodes P and Q, |P|=|Q|.



Left: A resistor phantom from Gagnon et al[7] with 350 resistors and 16 electrodes. Right: Illustrating that this network is well connected where P is the first 8 electrodes

Characterizing Transconductance for planar networks

We have the following characterization of transfer conductance matrices of well-connected planar networks[4].

Colin de Veriére's criterion

A symmetric matrix ${\bf A}$ is a transfer conductance matrix of a well connected planar network if and only if

$$(-1)^k \det \mathbf{A}_{P,Q} > 0, \tag{2}$$

where $\mathbf{A}_{P,Q}$ is the matrix restricted to subsets $P,Q\subset\{1,...,L\}$, $P\cap Q=\emptyset$, |P|=|Q|=k and on the circle the electrodes in P and Q are ordered as $p_1,...,p_k,q_k,...,q_1$.

The sets P and Q should be thought of as two ordered and not interleaved sets of electrodes.

Checks on 2D EIT data

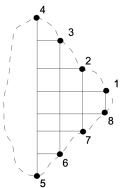
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- If an adjacent pair is driven the voltages are non-increasing between source and sink. This is a consequence of the condition we stated. It is often used to check electrodes are in the correct order.
- As this is a complete set of criteria any such transfer conductance can be realized as a resistor network. There is a canonical way to do this with only



n-port networks

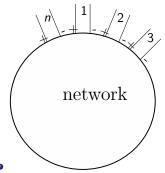
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Open circuit resistance

 The open circuit resistance matrix of this n-port network is the matrix S such that

$$V = SI \tag{3}$$

where here $\mathbf{I} \in \mathbb{R}^n$ is a current applied across each pair of terminals and $\mathbf{V} \in \mathbb{R}^n$ the resulting voltages across those terminals.

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• where ${\bf R}$ is the transfer resistance of the network with the L=2n>4 distinguished terminals and where the i-th column of the matrix ${\bf C}$ has a 1 in the row corresponding to the + terminal of the i-th port and -1 in the row corresponding to the - terminal and is otherwise zero.

Paramountcy

Cederbaum [1] noticed that the open circuit resistance matrix of an *n*-port has a property known as paramountcy.

Definition:

Let \mathbf{S} be real symmetric $n \times n$ matrix with elements s_{ij} . Let $I = (i_1, i_2, ..., i_k)$ be an ordered set k < n of indices between 1 and n and S_{II} the determinant of the submatrix of rows and columns indexed by I. Suppose J is another ordered subset of k indices and denote by S_{IJ} the determinant with rows indexed by I and columns by J. We say the matrix \mathbf{S} is paramount if $S_{II} \geq |S_{IJ}|$ for all such I and J.

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- As an example consider a 4-port where a current is driven in port 1, port 2 and 3 are short circuted and port 4 open circuted. resulting in

$$V_1 = s_{11}I_1 + s_{12}I_2 + s_{13}I_3$$

$$0 = s_{21}I_1 + s_{22}I_2 + s_{23}I_3$$

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Hence

$$\begin{vmatrix} V_1 & s_{11} & s_{12} & s_{13} \\ 0 & s_{21} & s_{22} & s_{23} \\ 0 & s_{31} & s_{32} & s_{33} \\ V_4 & s_{41} & s_{42} & s_{43} \end{vmatrix} = 0$$

and we have

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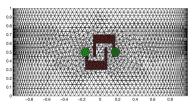
• and we see

$$|s_{44}/|s_{14}| > |V_1/V_4| \ge 1$$

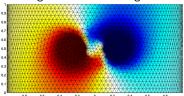
which is the condition of paramountcy.

3D transfer resistances that are not valid 2D ones

In 3D voltages on electrodes on a plane need not decrease monotonically source to sink.



An asymmetrical conductivity anomaly in cylindrical domain created using EIDORS and Netgen. Electrodes in green.



The equipotential lines on the surface resulting from driving current between the two circular electrodes. Note that in the plane through the electrodes that voltage is not monotonically decreasing from source to sink, see for example the isopotential between the yellow and white shading

References I



I. Cederbaum, Applications of matrix algebra to network theory, IRE Trans. Circuit Theory, vol. CT-3, 179-182,1956



E.B. Curtis, D. Ingerman and J.A. Morrow, Circular planar graphs and resistor networks, Linear algebra and its applications, 283, p115–150, 1998.



D Ingerman, J.A. Morrow, On a characterization of the kernel of the Dirichlet-to-Neumann map for a planar region, SIMA Vol. 29 Number 1 pp. 106-115 1998



Y. Colin de Verdière, Réseaux électriques planaires I, Publ. Inst. Fourier, V 225, p1-20, 1992.



Y. Colin de Verdière, I. Gitler and D. Vertigan, Réseaux électriques planaires II, Comment. Math. Helvetici 71, 144-167, 1996



W. R. B. Lionheart and K. Paridis, Finite elements and anisotropic EIT reconstruction, Journal of Physics: Conference Series, vol. 224, no. 1, p. 012022, 2010



H Griffiths, A phantom for electrical impedance tomography, Clin. Phys. Physiol. Meas., 9, 15-20, 1988.

References II



H. Gagnon *et al* A resistive mesh phantom for assessing the performance of EIT systems, IEEE T Biomed. Eng., 57:2257?2266, 2010.



J. Just *et al*, Constructing resistive mesh phantoms by an equivalent 2D resistance distribution of a 3D cylindrical object. Proceedings EIT Conference, Bath, 4-6 May, 2011.



A. Al Humaidi. Resistor networks and finite element models. PhD thesis, University of Manchester, Manchester, UK, 2011.



W.R.B. Lionheart and K. Paridis, Finite elements and anisotropic EIT reconstruction. Journal of Physics: Conference Series, 224, 2010.



W.R.B. Lionheart and K. Paridis, Determination of an embedding consistent with discrete Laplacian on a triangular graph, in preparation.