**SYSC 3203: Fall 2019**

**Lab 3A Report**

Submit this page to the lab instructor.

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**1: Filter Design**

1.1: Sketch the filter requirements (gain versus frequency) corresponding to the required specifications.

1.2: Using a Chebyshev filter design, what filter order is required to meet the specifications?

1.3: How many stages are required to implement this design using the Sallen-Key (VCVS) filter configuration (Figure 1)?

1.4: Using the values in Table 1, calculate the gain and real-world cutoff frequency fc required for each filter stage.

1.5: Choose suitable values for the components $R\_{1}$,$ R\_{2}$, $C\_{1}$,$ C\_{2}$, $R\_{3}$, $R\_{4}$ for each stage of your design.

**2: Filter Assembly and Test**

2.1: Sketch the circuit diagram for the Sallen-Key high pass filter.

2.2: Sketch a schematic for the Sallen-Key high pass filter, showing the chip layouts for the OP97 op-amps and labeling all of the terminals. Please label the testing points for your circuit.

2.3: What is the lowest frequency at which you can reasonably measure the filter response? What happens to the signal at very low frequencies?

2.4: From your measurements, calculate how much rejection (in dB) the filter provides at the 60Hz powerline interference frequency. Is this what you expect for a second-order filter?

2.5: Show proper operation of the high pass filter.

Verified: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date/Time:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_