CARLETON UNIVERSITY
Department of Systems and Computer Engineering

SYSC 3203
Project Title: EMG-Controlled Mouse
Milestone #3A: EMG signal filter / envelope detector

Raw EMG signals are often contaminated with DC and 60 Hz powerline interference signals. After rejecting the interference, the envelope (ie. shape) of the signal needs to detected. Milestone #3 consists of designing a filter adapted for measuring an electromyographic (EMG) signal such as the one coming out of the instrumentation amplifier designed in the previous lab.

EMG signals typically have a frequency range from a few tens of a hertz to a few kilohertz. Your task is to design a high pass filter (HPF) with the following specifications:

- Cut-off frequency: 180 Hz.
- > 40 dB rejection of 60 Hz powerline interference
- < 1 dB passband ripple

1. Filter Design

1.1: Sketch the filter requirements (gain versus frequency) corresponding to the specifications above.

1.2: Using a Chebyshev filter design, what filter order is required to meet the specifications?

Table 1: Sallen-Key filter design parameters

N	F_s*(40dB)*	F_s*(60dB)*	F_s *(80dB)*	f_n	*G*	f_n	*G*	f_n	*G*	f_n	*G*
FILTER = Chebyshev 0.5dB											
2	12.16	38.46	121.62	1.231	1.842						
4	2.57	4.47	7.85	0.597	1.582	1.031	2.660				
6	1.62	2.26	3.24	0.396	1.537	0.768	2.448	1.011	2.846		
8	1.35	1.66	2.11	0.297	1.522	0.599	2.379	0.861	2.711	1.006	2.913
FILTER = Chebyshev 2.0dB											
2	8.61	27.23	86.10	0.907	2.114						
4	2.21	3.76	6.61	0.471	1.924	0.964	2.782				
6	1.50	2.04	2.88	0.316	1.891	0.730	2.648	0.983	2.904		
8	1.27	1.55	1.95	0.238	1.879	0.572	2.605	0.842	2.821	0.990	2.946

The circuit of **Error! Reference source not found.** represents a Sallen-Key (VCVS) implementation of a second-order active HPF. In its simplest form with equal resistor and capacitor values i.e. $R_2 = R_1 = R$ and $C_2 = C_1 = C$, the response of the filter may be written in the form

$$T(\omega) = \frac{(j\omega CR)^2}{1 + (3 - G)j\omega CR + (j\omega CR)^2}$$

where the gain G is given by the usual non-inverting op-amp gain expression $G = 1 + R_4/R_3$.

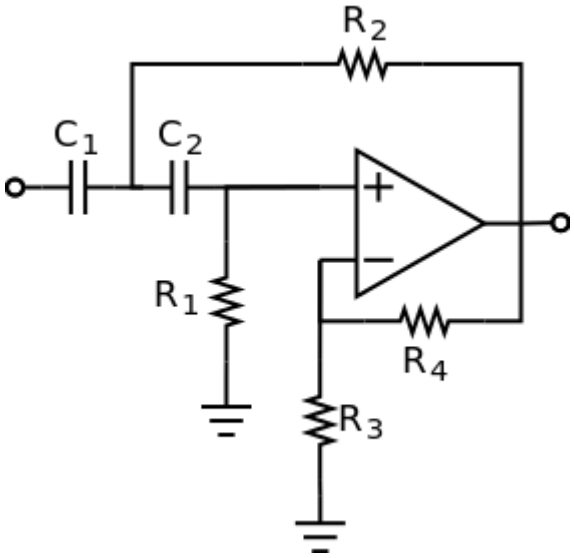

Figure 1: Sallen-Key active HPF implementation

1.3: How many stages are required to implement this design using the Sallen-Key (VCVS) filter configuration (Error! Reference source not found.**)?**

1.4: Using the values in Table 1, calculate the gain and real-world cutoff frequency f_c required for each filter stage.

1.5: Choose suitable values for the components $R_1, R_2, C_1, C_2, R_3, R_4$ for each stage of your design.

2. Filter Assembly and Test

Once you have answered the above questions, assemble your design using two OP97 amplifiers from your kit.

2.1: Sketch the circuit diagram for the Sallen-Key high pass filter.

2.2: Sketch a schematic for the Sallen-Key high pass filter, showing the chip layouts for the OP97 op-amps and labeling all of the terminals. Please label the testing points for your circuit.

Verify its operation using a function generator and an oscilloscope.

- Choose some frequencies at which to test the filter response – remember that you will want to test both the low frequencies ($\ll f_c$) and high frequencies ($\ll f_c$) but you should concentrate most of your measurement points in the frequency range where you expect the response to vary most rapidly versus frequency.
- At each of the chosen frequencies, measure the amplitude of the input signal and the amplitude of the output signal – you can do an *uncalibrated* measurement by splitting the input signal between Channel 1 of the oscilloscope and your circuit's input terminals, and comparing it with the output connected to Channel 2. *Think about how you would make a properly calibrated gain measurement*.

2.3: What is the lowest frequency at which you can reasonably measure the filter response? What happens to the signal at very low frequencies?

2.4: From your measurements, calculate how much rejection (in dB) the filter provides at the 60Hz powerline interference frequency. Is this what you expect for a second-order filter?

2.5: Show your testing results and assembled circuit to the instructor and have him/her fill and sign the instructor verification sheet.