SYSC-5807
METHODOLOGICAL ASPECTS OF MODELLING AND SIMULATION
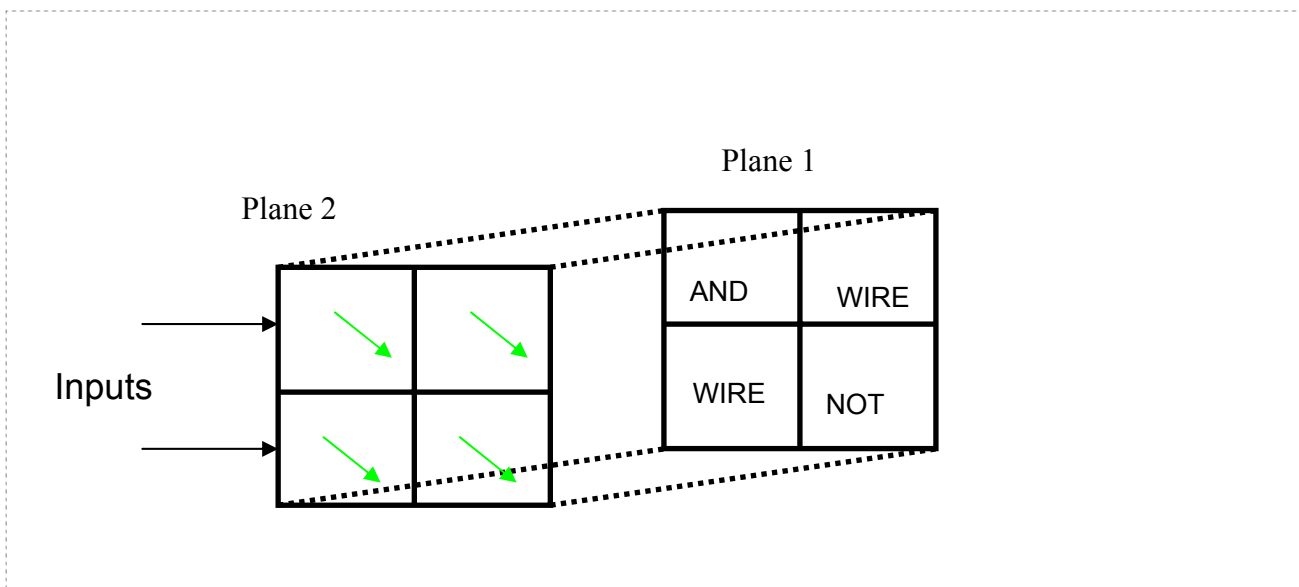
Estimation of Internal Power Dissipation in Glitching Using Cellular Automata

(Term Project)

Date: December 1, 2003.

Shanta Ramchandani
Student #: 100404100

PART 1 – CONCEPTUAL MODEL

The cell devs model implemented in this assignment is based on the model proposed in the article titled, "Estimation of Power Dissipation in Glitching Using Complex-Time Cellular Automata" by I. Karafyllidis, S.Mavridis, D.Soudris, and A.Thanailakis.

This particular model will consist of 2 Cell DEVS models coupled. The first model contains 3 planes. The first of which is a connectivity matrix and acts as a 'memory' to the second plane. The 3rd plane is a copy of the second plane so that the cells in the second plane can compare their new inputs to their previous inputs. The 2nd plane is the actual circuit and consists of 6 data inputs. Each cell in the 2nd plane refers to its corresponding cell in the first plane in order to determine its function (ie: AND, OR, NOT, WIRE).

Note : The (green) arrows are outputs to the second Cell DEVS model

The 2nd Cell DEVS model acts as a counter. Everytime a cell in the first model (2nd plane) changes state or if its inputs change state, an output is sent to the corresponding cell in the 2nd model. This cell increments its value by one everytime it receives an input. There is one cell in the 2nd model that calculates the total power dissipation every pre-determined time interval using the following equation:

$P_{total} = P_{quiescent} + (P_{active} \times \text{Total\_Number\_of\_Glitches})$
$= 1.3mW + (0.003mW \times \text{Total\_Number\_of\_Glitches})$

These values are supplied by the semiconductor vendors and vary for the logic families used. The assumption here is that the Motorola GigaBit Logic 10G GaAs is the logic family used and that every gate has the same $P_{quiescent}$ and P_{active}.

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PART 2 – FORMAL SPECIFICATIONS AND SIMULATION STRATEGIES

Coupled Cell-DEVS -- CIRC

Xlist = { φ }

Ylist = { (0,0,1), (0,1,1), (0,2,1), (0,3,1), (0,4,1), (0,5,1), (1,0,1), (1,1,1), (1,2,1), (1,3,1), (1,4,1), (1,5,1), (2,0,1), (2,1,1), (2,2,1), (2,3,1), (2,4,1), (2,5,1), (3,0,1), (3,1,1), (3,2,1), (3,3,1), (3,4,1), (3,5,1), (4,0,1), (4,1,1), (4,2,1), (4,3,1), (4,4,1), (4,5,1), (5,0,1), (5,1,1), (5,2,1), (5,3,1), (5,4,1), (5,5,1) }

I   = $<P^x, P^y>$ with P^x = { φ } and
       P^y = { <Y(0,0,1), 1> , <Y(0,1,1), 1> , <Y(0,2,1), 1> ... <Y(5,3,1), 1> , <Y(5,4,1), 1> , <Y(5,5,1), 1>}

X = {dataIn1, dataIn2, dataIn3, dataIn4, dataIn5, dataIn6}

Y = {out1, out2, out3, ..., out34, out35, out36}

N = { (-1,-1,0), (-1,0,0), (-1,1,0), (0,-1,0), (0,0,0), (0,1,0), (1,-1,0), (1,0,0), (1,1,0), (0,0,-1),
     (-1,-1,1), (-1,0,1), (-1,1,1), (0,-1,1), (0,0,1), (0,1,1), (1,-1,1), (1,0,1), (1,1,1) }

m = 6 ; **n** = 6

B = { φ }

C = { (0,0,0)…(5,5,0), (0,0,1)…(5,5,1), (0,0,2)…(5,5,2) }

select = <dataIn1, dataIn2, dataIn3, dataIn4, dataIn5, dataIn6>

Coupled Cell-DEVS -- POWERCALC

Xlist = { (0,0), (0,1), (0,2), (0,3), (0,4), (0,5), (1,0), (1,1), (1,2), (1,3), (1,4), (1,5), (2,0), (2,1), (2,2), (2,3), (2,4), (2,5), (3,0), (3,1), (3,2), (3,3), (3,4), (3,5), (4,0), (4,1), (4,2), (4,3), (4,4), (4,5), (5,0), (5,1), (5,2), (5,3), (5,4), (5,5) }

Ylist = { φ }

I   = $<P^x, P^y>$ with P^x = { <X(0,0), 1> , <X(0,1), 1> , <X(0,2), 1> ... <X(5,3), 1> , <X(5,4), 1> , <X(5,5), 1>}
       and P^y = { φ }

X = {in1, in2, in3, ..., in34, in35, in36}

Y = { φ }

N = { (-3,-3), (-3,-2), (-3,-1), (-3,0), (-3,1), (-3,2), (-3,3), (-2,-3), (-2,-2), (-2,-1), (-2,0), (-2,1), (-2,2), (-2,3),
 (-1,-3), (-1,-2), (-1,-1), (-1,0), (-1,1), (-1,2), (-1,3), (-0,-3), (0,-2), (0,-1), (0,0), (0,1), (0,2), (0,3), (1,-3), (1,-2),
(1,-1), (1,0), (1,1), (1,2), (1,3), (2,-3), (2,-2), (2,-1), (2,0), (2,1), (2,2), (2,3), (3,-3), (3,-2), (3,-1), (3,0), (3,1),
(3,2), (3,3)}

Shanta Ramchandani
Student #: 100404100

m = 7 ; **n** = 7

B = { φ }

C = { (0,0)…(6,6) }

select = <in1, in2, in3, in4, in5, … , in33, in34, in35, in36>

External Coupling Definition

X = {dataIn1 $_{circ}$, dataIn2 $_{circ}$, dataIn3 $_{circ}$, dataIn4 $_{circ}$, dataIn5 $_{circ}$, dataIn6 $_{circ}$ }

Y = { φ }

D = { circ, powerCalc }

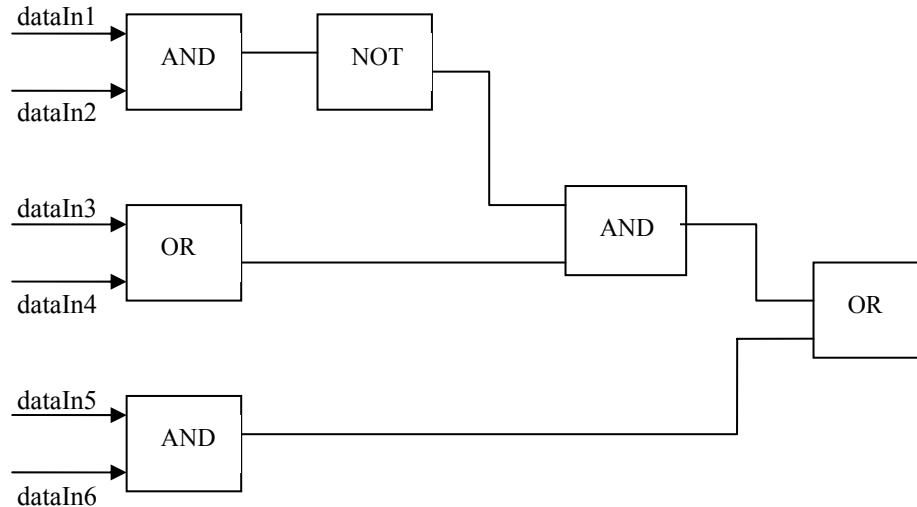**I**$_{circ}$ = powerCalc

I$_{powerCalc}$ = circ

Z$_{circ/powerCalc}$: circ(0,0,1) → powerCalc(0,0)
circ(0,1,1) → powerCalc(0,1)
circ(0,2,1) → powerCalc(0,2)
circ(0,3,1) → powerCalc(0,3)
…
circ(5,3,1) → powerCalc(5,3)
circ(5,4,1) → powerCalc(5,4)
circ(5,5,1) → powerCalc(5,5)

select = < circ, powerCalc >

* Variation: The above External Coupling scheme is what should be. Since there are issues when connecting more than one output of a Cell-DEVS to the inputs of another Cell-DEVS models, a buffer with no delay was introduced. One buffer for each output from the first Cell-DEVS.

Shanta Ramchandani
Student #: 100404100

SIMULATION STRATEGY AND RESULTS

The following circuit is what has been implemented in this simulation. The design is somewhat dynamic in that different circuits can be implemented by modifying the circuit.VAL file.

The following inputs were used to exercise the model:
The inputs to dataIn-1-6] circuit alternate between 0 and 1:

```
00:00:01:020 dataIn1 1
00:00:01:020 dataIn2 1
00:00:01:020 dataIn3 1
00:00:01:020 dataIn4 1
00:00:01:020 dataIn5 1
00:00:01:020 dataIn6 1

00:00:02:020 dataIn1 0
00:00:02:020 dataIn2 0
00:00:02:020 dataIn3 0
00:00:02:020 dataIn4 0
00:00:02:020 dataIn5 0
00:00:02:020 dataIn6 0

00:00:03:020 dataIn1 1
00:00:03:020 dataIn2 1
00:00:03:020 dataIn3 1
00:00:03:020 dataIn4 1
00:00:03:020 dataIn5 1
00:00:03:020 dataIn6 1

00:00:04:020 dataIn1 0
00:00:04:020 dataIn2 0
00:00:04:020 dataIn3 0
00:00:04:020 dataIn4 0
00:00:04:020 dataIn5 0
00:00:04:020 dataIn6 0

00:00:05:020 dataIn1 1
00:00:05:020 dataIn2 0
```

Shanta Ramchandani
Student #: 100404100

```
00:00:05:020 dataIn3 1
00:00:05:020 dataIn4 0
00:00:05:020 dataIn5 1
00:00:05:020 dataIn6 0

00:00:06:020 dataIn1 0
00:00:06:020 dataIn2 1
00:00:06:020 dataIn3 0
00:00:06:020 dataIn4 1
00:00:06:020 dataIn5 0
00:00:06:020 dataIn6 1
```

The results can be viewed with the CD++ Modelor tool by loading the *circuit_mod.drw* file.
** The simulation generates a *circuit.drw* file. The *circuit_mod.drw* contains one plane of the *circuit.drw* file. This has been done for ease of viewing in the CD++ Modelor tool.

The *powerCalc.drw* file can be viewed and shows where the logic gates are distributed in the 'chip' and the top right corner cell contains the total internal power dissipation.

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