Simulation of Anisotropic Etching of Monocrystalline Silicon with Cell-DEVS

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ABSTRACT: *Anisotropic etching is widely used in semiconductor manufacture industry and some other areas. In order to reduce the cost and shorten the producing period of a new product, manufacturers usually build appropriate models to simulate the manufacturing procedure and results. DEVS model and Cell-DEVS model is a popular way for building models and executing simulations. In this paper, we simulate the anisotropic etching of monocrystalline silicon by building Cell-DEVS model with extended C++ language. We analysis the process of etching and rebuild it with the REST version of software. In addition, we refine our model with more states and multiple ports, and the result is more close to the reality.*

Keywords
Anisotropic wet etching; Cell-DEVS; monocrystalline silicon; crystal.

1. Introduction

Wet Etching is the process of using strong acid or other methods to cut into the unprotected part of a material. In semiconductor manufacture industry, the etching of silicon is widely and frequently used. For example, MEMS (Micro-Electro-Mechanical Systems), a new technology, which is combined with microelectronics and mechanical engineering, uses etching technique to fabricate different kinds of structures on the surface of silicon wafers. Those structures could be cantilever beam, which is part of a new kind of resonator, or even vibrating structure used for MEMS gyroscope.

1.1 Etching Classification

Etching techniques could be classified into two major categories: wet etching and dry etching. The major difference between them is that the wet etching uses solution or solvent to etch the target material. Considering the manufacturing and testing of a structure or circuit on the wafer, which may require much higher cost and suffer for failure with higher possibility, a good simulation design is strongly needed. Also, this kind of simulation can help to reduce the research cost and shorten the research period.

Except for the etching material, etching techniques could also be classified into anisotropic etching and isotropic etching, based on the etched material characteristics.

The difference is that, in anisotropic etching, the etching rate varies in different crystallographic direction, while in isotropic etching the etching rate is stable to different directions.

1.2 Crystal Structure

Referring to the research in Solid State Physics, the crystal could be considered to be constructed by numbers of cells which are totally the same with each other. Those cells could be treated as the repetitions of the same basic cell, which refers to as structure cell or unit cell. Solid State Physics uses Miller System to study the structure of crystals. In this system, a crystallographic direction is basically a vector between two points in the crystal, and a crystallographic plane is a plane formed by different atoms. And because the structure of crystal is periodically repeated, the crystallographic plane is actually a set of planes which are parallel to each other. Using Miller indices to represent the crystallographic directions and the crystallographic planes, some examples are shown in Figure 1.

The crystal structure of Monocrystalline Silicon is called diamond structure, as shown in Figure 2. The dark dots represent atoms of some certain crystal, and the lines (except for the lines form the cube) stand for the chemical bonds between each atom pair. Every atom is connected with other four atoms by covalent bonds. A Monocrystalline Silicon wafer is structured by periodically repeating the structure shown in figure 2.

As the anisotropic wet etching is widely used in semiconductor manufacturing industry and some other areas, in our simulation, we simulate Si wet etching process by using Cell-DEVS. Wet etching is the process of using chemical reaction between some special liquid and wafer to remove the part uncovered by the photoresist. Since wet etching is a pure chemical process, it has advanced selectivity which stops at current thin-film without affecting other material.

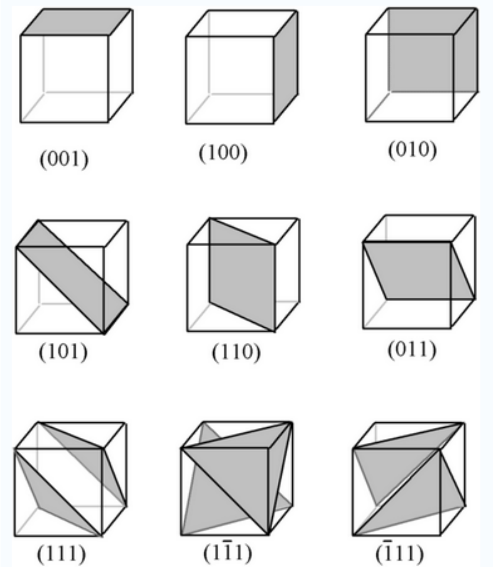


Figure 1 *Examples of different planes indicated by Miller indices*

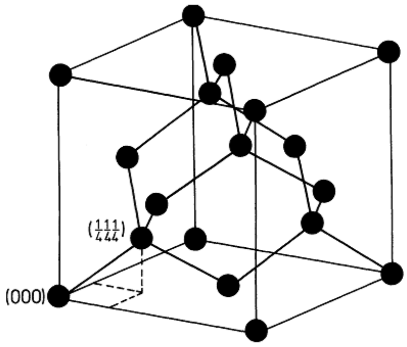


Figure 2 *Diamond crystal structure*

In Si wet etching, the etching speed appears to be different with different crystal planes. Although the exact mechanism is not discovered, but, according to the experimental results, (111) plane density is larger than the (100) plane, so the etching speed of (111) plane will be lower than that of (100) plane. In application, if the Si on (100) plane is covered by SiO_2 with certain pattern, the directional etchant will generate an accurate V slot with border being (111) plane and angle being 54.7 degree with (100) plane, as showed in Figure 3.

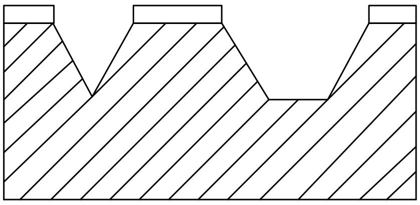


Figure 3 *V slot of (100) plane and (111) plane*

Our simulation is to reproduce the whole process of forming V slot in Cell-DEVS simulate the complex physical model into cell space model, which is required to be time discrete, space discrete and state discrete. Considering from the Si stereochemical structure, each Si atom can be seen as a cell and they are distributed discretely in Si molecule. For detailed illustration of Si etching process with Cell-DEVS, we describe in the following.

1.3 Cell-DEVS Tool with CD++

Cell-DEVS with CD++ is an advanced simulation tool, which is used to perform the cell atomic module behaviors with some programming. As Figure 4 shows, the Cell DEVS module can be divided into atomic module and coupled module, and every cell is regarded as a basic atomic module. In default, each cell has one input port *neighborChange* and one output port *out*, which limits the input/output path of a cell.

To perform the cell behavior, operations and functions are required in Cell-DEVS tool with CD++. In specific, it includes the basic logic operations: AND OR NOT XOR IMP and EQV, the basic arithmetic operations: + - * /, and the comparison between any two numbers: > >= < <= = != as well as many functions used for executing different tasks. It's worth noting that some functions are predefined to provide the number of neighbor state, such as: *statecount truecount falsecount.* For example, *statecount(1)* means the number of neighbors with state being 1; and we can use such function to differentiate each cell. For more information, please see the Reference [1], CD++ user's manual.

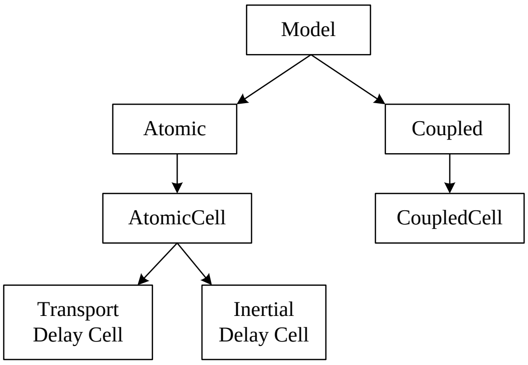


Figure 4 *Model hierarchy*

In our simulation, we use a new version of software: RETS, which is the extent of prior version with adding multiple ports and state variables. By supporting multiple variable states, multiple planes are not used to realize multiple states, but to define more complex phenomenon. That means, each of the planes can include cells with more than one state. Keywords: *StateVariables*, *StateValues* and *InitialVariableValue* are required to define. Another verification is the number of port isn't fixed any more. As with the increase of module complexity, only one pair ports are not enough. Supporting multiple port number allows us to send message out to and receive message from the external module in different neighbor ports. Keyworkd: *NeighborPorts* is required here. For more information, please see the Reference [2], user's manual.

As the RETS version software is nonlocal, a file named ***.xml*** is required to configure the module running environment. Reference [3] gives a detailed running and configuration methods, and we won't illustrate more in this paper.

2. 3D Model Specification

2.1 Conceptual Model

Before etching process, we should understand the basic information about Si atom structure. Actually, Si atom can connect with each other in covalent bond, as showed in Figure 5. Wafer is composed of a large number of such Si atom and connected with covalent bond. On the base of basic Si atom structure, we can divide wafer into many layers with four different layers as a cycle, others are just repeat such four layers.

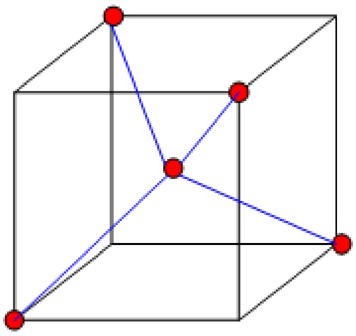
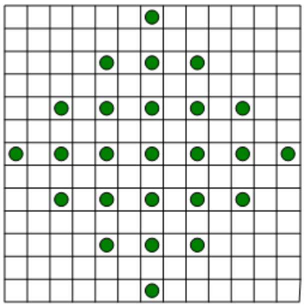
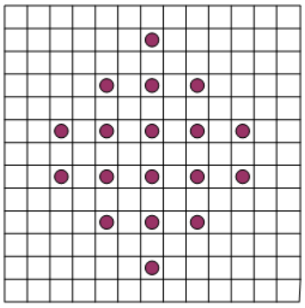


***Figure 5** Si atom and its direct neighbors*

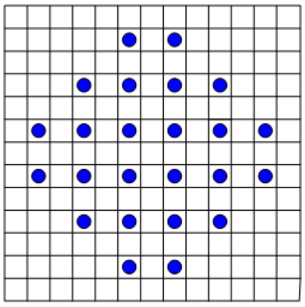
Follows are the platform of layers of atoms (shown in Figure 6), in the substrate, each unit cell of silicon can be divided in 5 layers, and we repeat every 4 layers, when arranged in periodic lattice. That means, the first layer has the same platform with the fifth layer. The specific layers are indicated as follows:



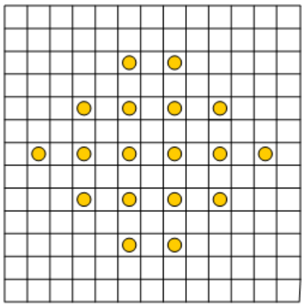
Layer1



Layer 2



Layer 3



Layer 4

***Figure 6** General view of different layers*

As we only highlight some atoms in each layer to see their difference, the actual model is that Si atoms are distributed in the whole plane. Observing the above figures, we know that layer 2 is layer 1 translating a line downward, layer 3 is layer 1 translating a line downward and translating a column to the right, while the layer 4 is layer 1 translating a column to the right. These platforms are correspond to [110] direction, and [100] direction could be seen after rotating these platforms for 45°. And we also assume that in lateral dimensions the atom layers are infinite. Each atom has four bonds, each one of the bonds may have two different states, one is complete and the other one is incomplete. And we could regard the atoms at the other side of the bonds as the neighbors of this atom. Incomplete bond means there are no atoms connect to this atom and complete bond means the opposite. So the atoms located in different crystallographic planes will have the structures indicated in Figure 7 (yellow means no atom; light green means the atom is exposed to solution, or, in other words, on the surface; dark green means the atom is located within the substrate and not exposed to the solution.)

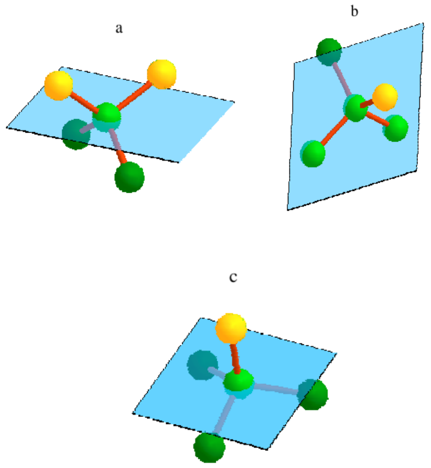


Figure 7 *Atomic bonding in (a) plane (100) (b) plane (110) and (c) plane (111)*

2.2 Cell-DEVS Formal Specifications

As Si structure is complex with four covalent bonds each Si atom, we consider is as a cube as simple. Showed in Figure 8, the central black cube is the considering cell, and it has 27 neighbors in total. During the etching process, all its neighbors' states should be put into consideration.

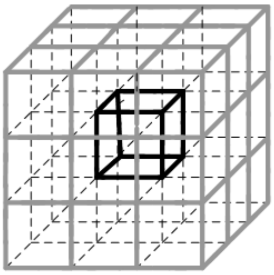


Figure 8 *Si cell neighborhood structure*

So the Cell_DEVS formal specification can be written as:

CD = <X, Y , I ,S, θ, N, δint , δext , τ, λ, D >

X = φ,

Y = φ,

I = < η, Px, Py >,

where

η = 27,

Px = { neighborChange, atom, expose },

Py = { out, atom, expose},

θ**= { (s, phase, f, σ), s ϵ S = { 0, 1, 2 }, phase ϵ {active, passive}, σ = 100 },**

S = { life, atom, mask, uncover }

Where

life = 0: atom is etched,

life != 0: atom isn't etched,

atom = 0: there is no atom in the cell

atom = 1: there is an atom in the cell

atom = 3: this cell is located in window area

mask = 0: cell is not located in mask area

mask = 1: cell is located in mask area

uncover = 0: the cell is exposed to solution

uncover = 1: the cell is not exposed to solution

N = { (-1, -1 ,1) (-1, 0, 1) (-1, 1, 1)
(0, -1, 1) (0, 0, 1) (0, 1, 1)
(1, -1, 1) (1, 0, 1) (1, 1, 1)

(-1, -1, 0) (-1, 0, 0) (-1, 1, 0)
(0, -1, 0) (0, 0, 0) (0, 1, 0)
(1, -1, 0) (1, 0, 0) (1, 1, 0)
(-1, -1, -1) (-1, 0, -1) (-1, 1, -1)
(0, -1, -1) (0, 0, -1) (0, 1, -1)
(1, -1, -1) (1, 0, -1) (1, 1, -1) },
D = transport delay 100ms,

2.3 Etching Rule Definition

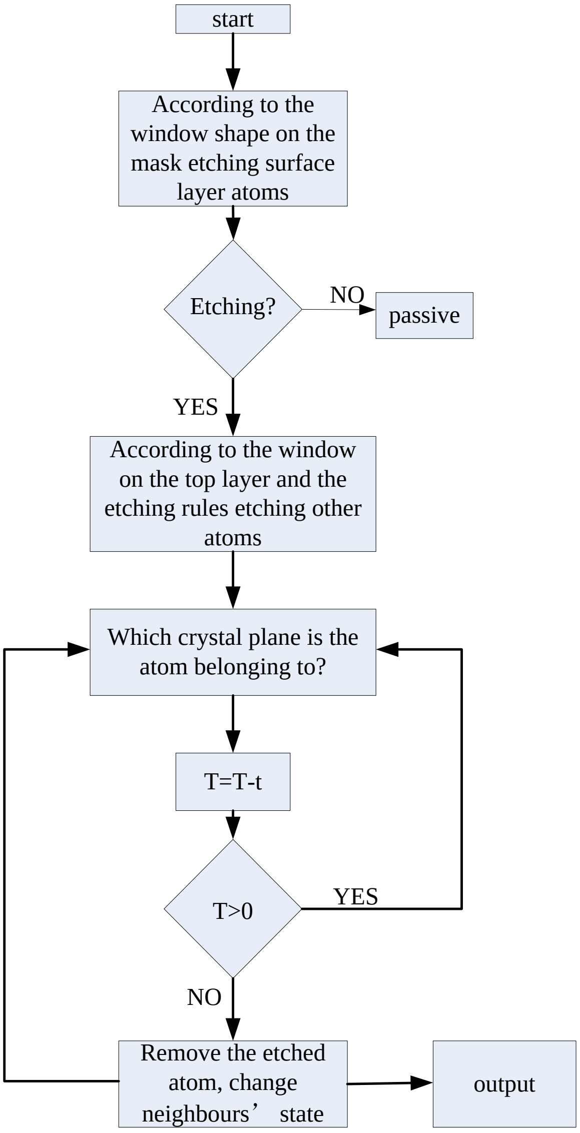

start
According to the window shape on the mask etching surface layer atoms
Etching?
NO
passive
YES
According to the window on the top layer and the etching rules etching other atoms
Which crystal plane is the atom belonging to?
T=T-t
T>0
YES
NO
Remove the etched atom, change neighbours' state
output

Figure 9 *brief flow-process diagram*

Figure 9 is the flow chart of etching process, from which we can have a clear view of how our simulation model work. In the first step is checking the window shape, because different shape will get different result. Once deciding the window shape, rule decides which cell should be etched and which not. If a cell should be etched, the atom in this cell will be removed based on the rule. When etching begins, the crystal plane is exposed and because of the different etching velocity in plane <110> <100> and <111>, we need to compute their etching time. At last, the atom in the cell will be etched and output the result, which is the effect to the neighbors.

The detailed rule as follows:

Rule 1 *: for every cell, if state atom = 1, state life = 1 and port atom = 1, the port atom become 2 after a delay ;*

Rule 2 *: for every cell, if state atom = 0, state life = 1 and port atom = 1, the port atom become 0 after a delay ;*

Rule 3 *: for every cell, if state atom = 3, state life = 1 and port atom = 1, the port atom become 3 after a delay ;*

Rule 4 *: for every cell, if state mask = 1 and port expose = 1, the port expose become 0 after a delay ;*

Rule 5 *: for every cell, if state atom = 0, the number of neighbor with port atom being 2 is less than 5 and port expose = 1, the port atom become 2 and port expose become 2 after a delay ;*

Rule 6 *: for every cell, if port atom is 0, the number of neighbor with port atom being 2 is less than 7 and state uncover is 1, state mask is 0port expose = 1; the port atom will become 3 and port expose become 0, also, the state uncover become 0 and state life become 0 after a delay ;*

Rule 7 *: for every cell, if port atom is 0, the number of neighbor with port atom being 2 is less than 7 and state uncover is 1, state mask is 0, port expose = 1; the port atom will become 3 and port expose become 0, also, the state uncover become 0 and state life become 0 after a delay ;*

Rule 8 *: for every cell, if port atom is 2, port expose is 2, the number of neighbor with port atom being 2 is less than 3 and state life is larger than 0, state mask is 0; the port atom will become 3 and port expose become 0 after a delay ;*

Rule 9 *: for every cell, if port atom is 2, port expose is 2, the number of neighbor with port atom being 2 is 3 and state life is larger than 0, state mask is 0; the port atom will become 3 and port expose become 0 after a delay ;*

Rule 10 *: for every cell, if port atom is 2, port expose is 2, the number of neighbor with port atom being 2 is 4 and the number of neighbor with port expose being 2 is larger than 1, state life is larger than 0, state mask is 0; the port atom will become 3 and port expose become 0 , state life will become 0 after a delay ;*

Rule 11 *: for every cell, if port atom is 2, port expose is 2, the number of neighbor with port atom being 2 is 4 and the number of neighbor with port expose being 2 is 1, state life is larger than 0, state mask is 0; the port atom will become 3, port expose become 0 and state life will become 0 after a delay ;*

Rule 12 *: { } { $life := $life ; $atom := $atom ; $mask := $mask ; $uncover := $uncover ; } 0 { (0,0,0) = 1 }*

Rule 13 *: { } 0 { t }*

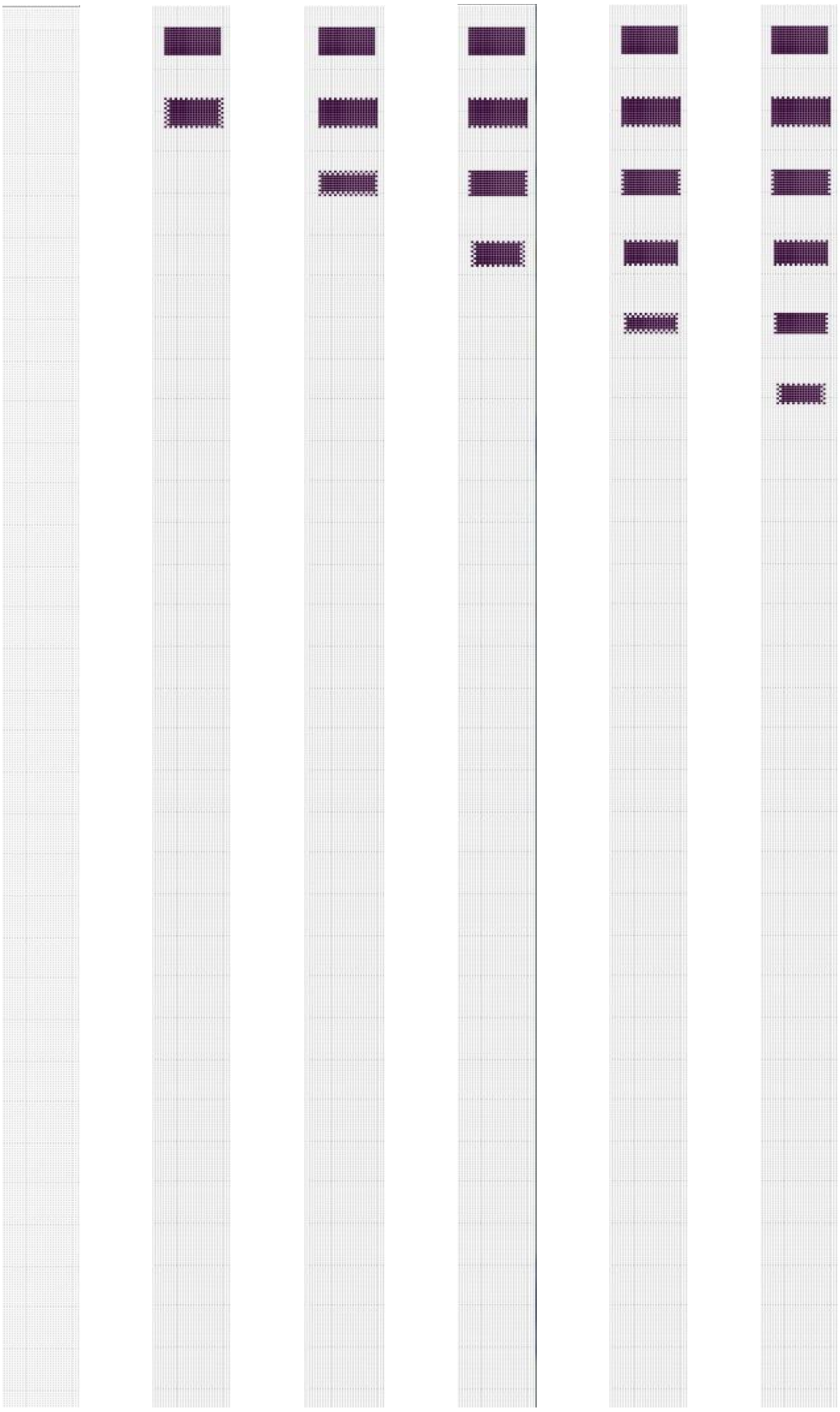
Specifically speaking, Rule 1 and Rule 2 uses additional state variables and the initial port value to find out if there is an atom in the cell, if there is an atom, the atom port value will be 2, if there is not, the value will be 0. Rule 3 specifies the window area, cells located in window area will have an initial state variable atom equals to 3, while other areas have the same variable with an initial value of 1 or 0. Rule 5 sets expose port value to 2 for those cells have atoms exposed to solution and are going to be etched immediately. Rule 4 specifies the mask areas which will never be etched during the simulation. Rule 11 tells that which crystallographic plane an atom belongs to and etch the atom using appropriate etching rate. The final two rules are used for initialization and the magic line.

3. Result and Analysis

We simulate the etching process of three different window shapes: *Rectangle, Square* and *Cross.* So, our simulation design has more powerful in proving the rules defined can etch the Si atoms with different shapes. For detailed result and analysis, please see the following.

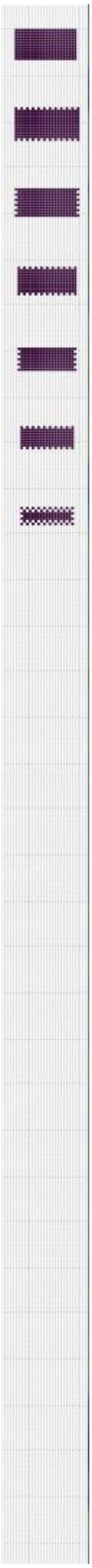
Rectangle

T1=00:00:100 T2=00:00:200 T3=00:00:300 T4=00:00:400 T5=00:00:500 T6=00:00:600

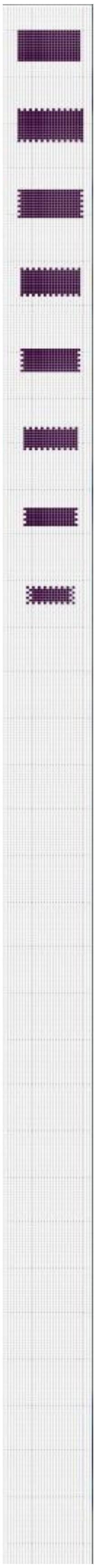


Rectangle

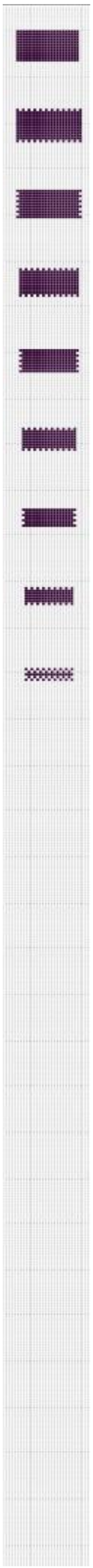
T7=00:01:000



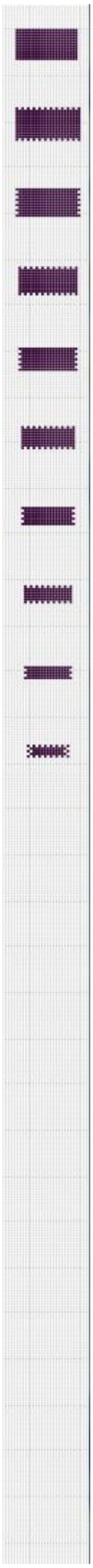
T8=00:01:100



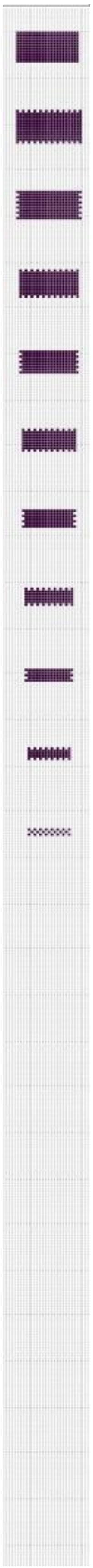
T9=00:01:200



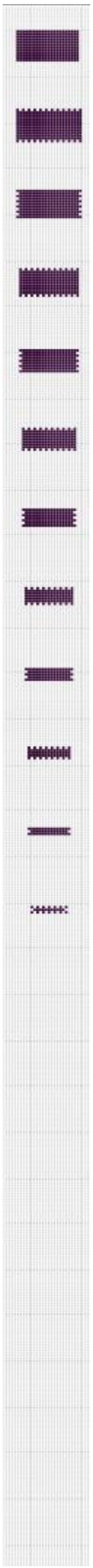
T10=00:01:300



T11=00:01:400



T12=00:01:500



The above 12 figures show the etching process of rectangle window from T1 to T12. The range of the rectangle is 30*30 and the layer ranks from top to the bottom as the mask to the 11th layer. The purple area represents the planes has been etched while the white area represents the planes with complete atom structure. Figure at T1 provides the initial state of Si atoms, means the complete crystal structure. After a time interval, the first layer has been etched as the mask shape and the etching process continue with time goes by.

When compared with the figure in Time = 00:00:000, the atoms in layer 1 and 2 here change. Following the rule 6 defined before:

Rule 6 *: for every cell, if port atom is 0, the number of neighbor with port atom being 2 is less than 7 and state uncover is 1, state mask is 0port expose = 1; the port atom will become 3 and port expose become 0, also, the state uncover become 0 and state life become 0 after a delay ;*

The port atom is 3 means the cell is in the window area, so this area will begin to etch while the surroundings are kept remained because of mask protection.

There are two important points here, 1). The unsmooth edge of each rectangle is because plane <111> is also into consideration, which is ignored in our Assignment 2. However, the effect of plane <111> is not clear, and the more obvious result please refers to the shape of Square and Cross. 2) The etching always begin with the edge, that is because the effect of neighbor atom number and the rule sequence, we let the bigger neighbor atom number do first, and then processing the cell with smaller neighbor atom number.

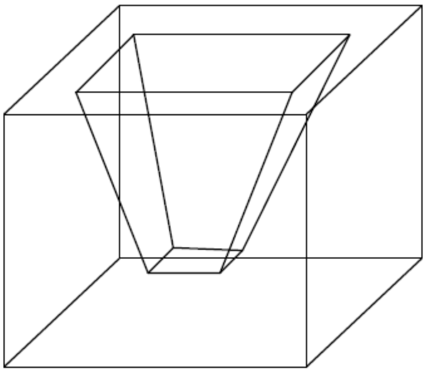
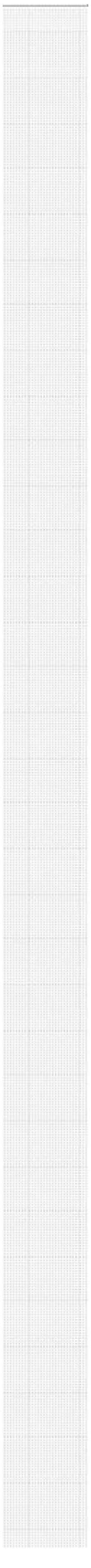


Figure 10 *Rectangle etching finish plan*

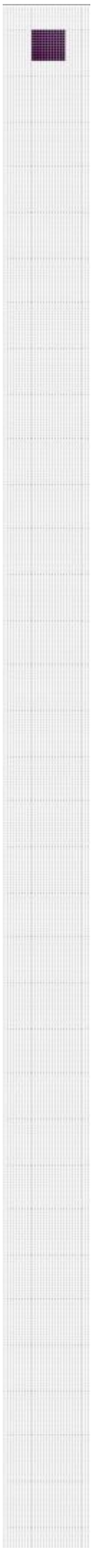
As we defined, the range of etched atoms decrease with the increase of layer number, through which we can get the expected V slot. This is showed in 2D visualization, and by overlapping them together layer to layer we can get an obvious etching process from top to bottom. As figure 10 shows, the final result should form a slot with the area of rectangle decrease with the increase of layer number.

Square

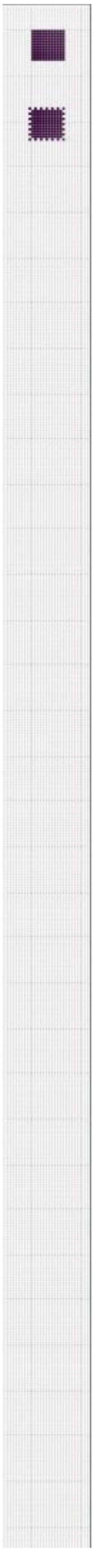
T1=00:00:000



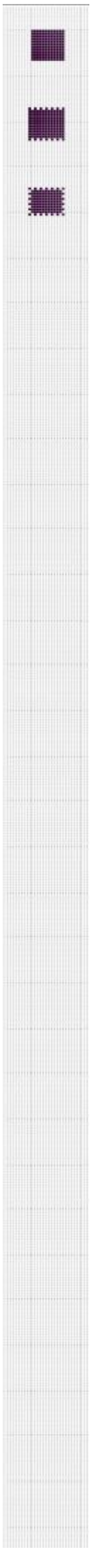
T2=00:00:100



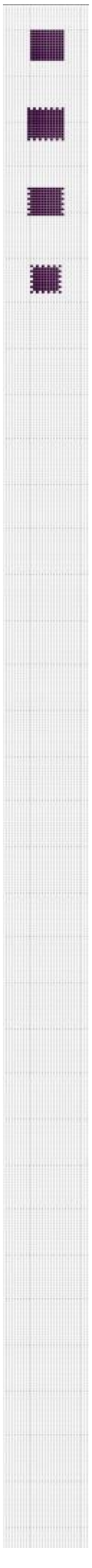
T3=00:00:200



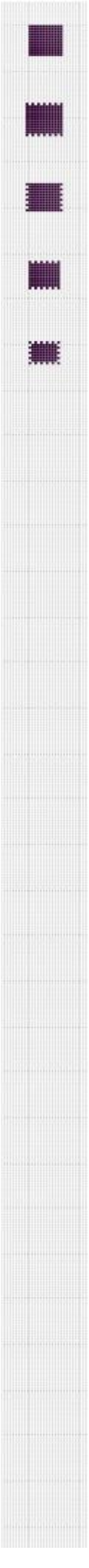
T4=00:00:300



T5=00:00:400

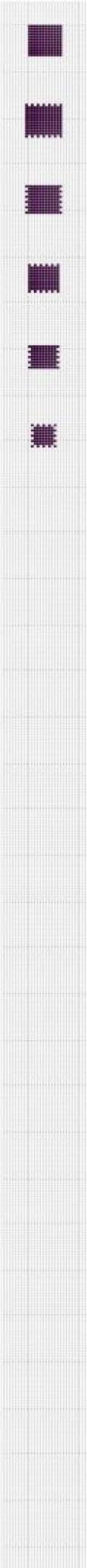


T6=00:00:500

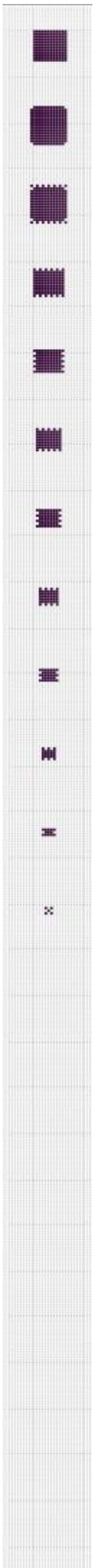


Square

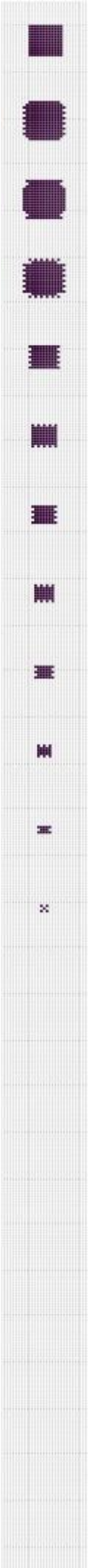
T7=00:00:600



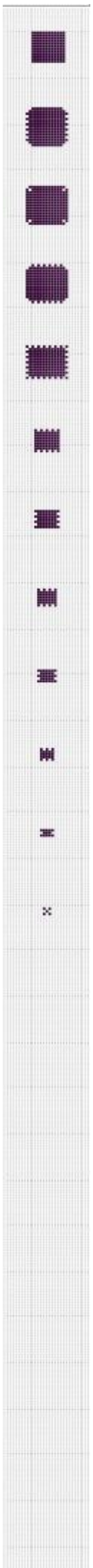
T8=00:01:000



T9=00:01:100

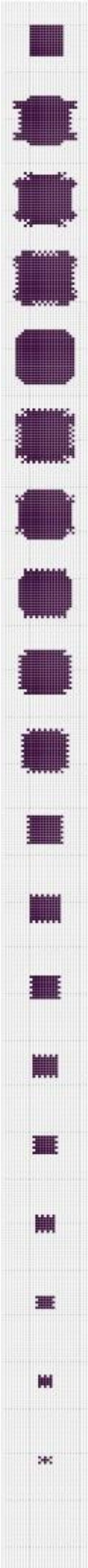


T10=00:01:200



…

T23=00:01:400



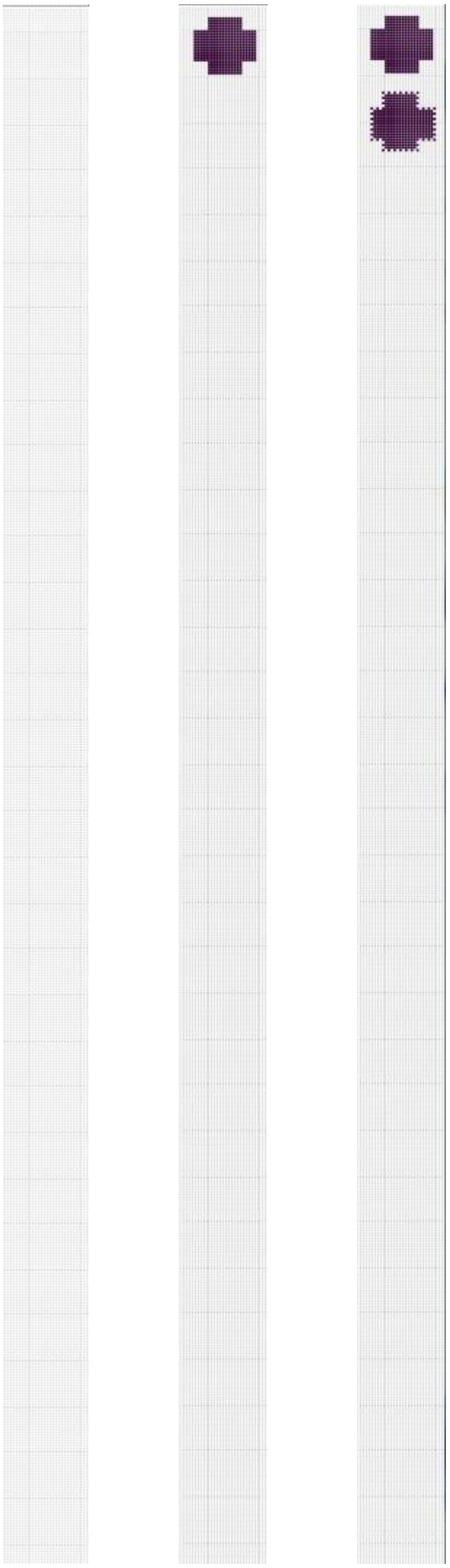
From the above figures we can have a general view of the etching process with window shape being square. The range of the square is 12*12 and the layer ranks from top to the bottom as the mask to the 11th layer. The purple area represents the planes has been etched while the white area represents the planes with complete atom structure. At T1, no atom is etched as the initially defined. At T2, the first layer is etched following the shape of mask, and it is etched layer by layer with goes by.

T7 to T12 follows the prior etching process (T1 to T6), and we can have a clearly view that a new layer will be etch after a time interval, which matches our defined rules exactly. It’s worth noting that the edge of each square isn’t smooth, that is because the effect of etching of crystal plane <111>. At the last time T12, the etching of square is finished and the 3D view can be gotten by overlapping each layer together.

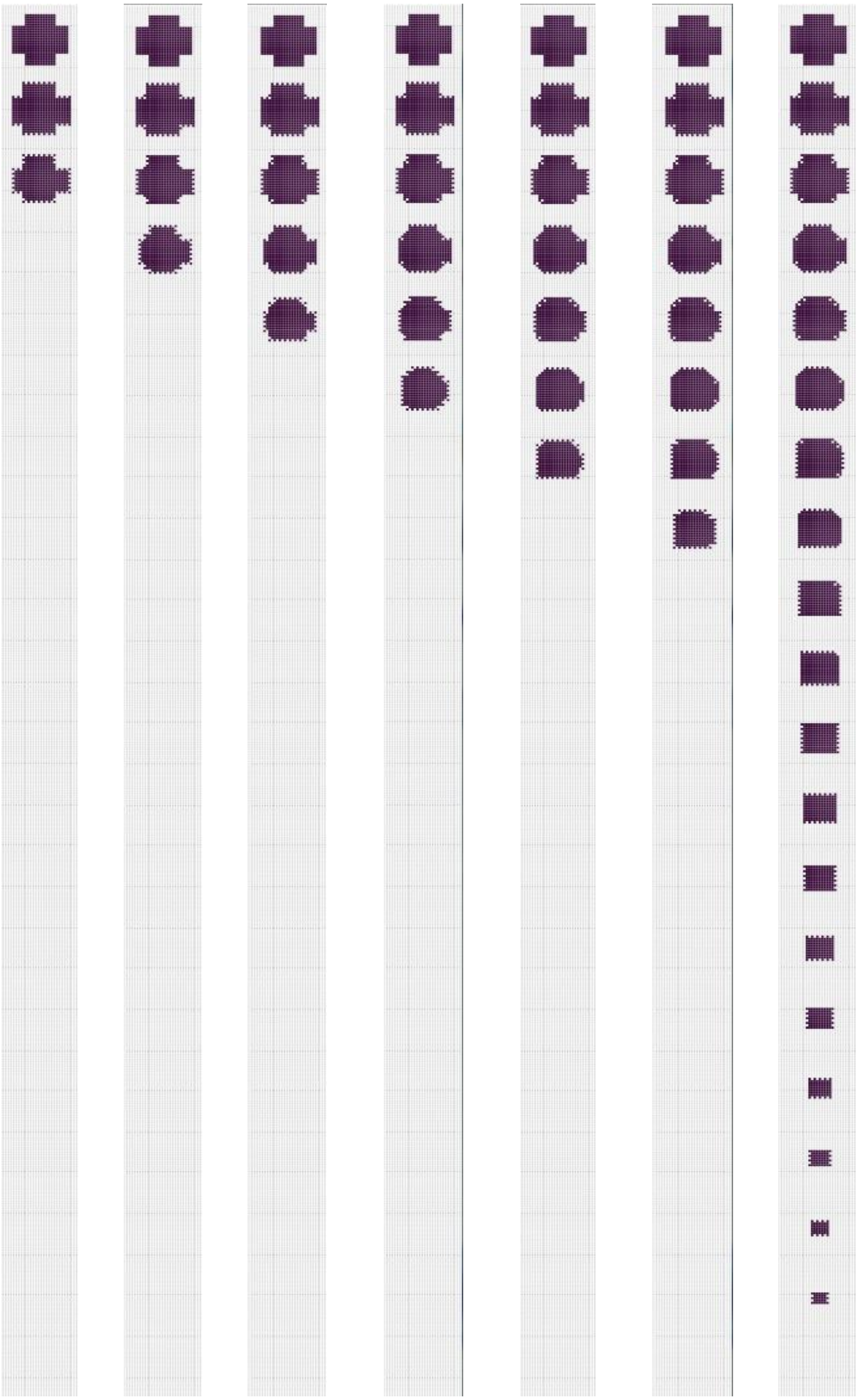
When analyzing the effect of plane <111>, we should know that the etching velocity is different at each plane. For simplicity and directly, we consider the rate between three planes are: <100>:<110>:<111> = 1:1:100. In such case, when plane <100> and <110> are etched at first, the plane <111> can keep the same, this is why there is a clear square at T2. But when time goes by, the plane <111> begins to etch, which will also affect the shape of etched before. In general, the edge atom suffers etched in plane <100> and <110> firstly and etched in plane <111> then. Through such ways, the square become unclear begin with edge, as showed in figure at T23 in the above figures.

Cross

T1=00:00:000 T2=00:00:100 T3=00:00:200



Cross



T4=00:00:300 T5=00:00:400 T6=00:00:500 T7=00:00:600 T8=00:01:000 T9=00:01:100 T21=00:03:100

For the Cross window shape etching, the process is more complicated than the other two, because the etching of plane <111> will remove the four edge atoms and shape will become square with time goes by. Please see the above figures, similar to the other two, The purple area represents the planes has been etched while the white area represents the planes with complete atom structure. At T2, we can see a clear cross shape, but when observing the figures at T3 to T6, the under layer etching area cannot keep the cross any more, illustrating when etching a new layer, the etched layer before doesn't keep the same but still be in etching. As the effect of etching plane <111>, the four ends of cross become obscured and change to the square finally, as showed in figure at T21.

When analyzing the effect of plane <111>, we should know that the etching velocity is different at each plane. For simplicity and directly, we consider the rate between three planes are: <100>:<110>:<111> = 1:1:100. In such case, when plane <100> and <110> are etched at first, the plane <111> can keep the same, this is why there is a clear cross at T1. But when time goes by, the plane <111> begin to etch, which will also affect the shape of etched before. In general, the edge atom suffers etched in plane <100> and <110> firstly and etched in plane <111> then. Through such ways, the cross become unclear begin with edge and become to the shape square at last, as showed in figure at T21.

Acknowledgement

We have learned a lot in finishing this paper and doing the programming, and we get a lot of help from Professor Gabriel. He provides us many new ideas and points in constructing the simulation module. Of course, partner is very important because we are a group to do the final project. We have to learn how to communicate and discuss with each other during the project, which plays an important role in developing ourselves. So, we want to say thank you to our professor, to the partner and to our school.

4. Conclusion

In our simulation, we regard Si etching as a Cellular Automata, which is discrete in time, space and state. Applying CD++ to simulate the Si wet etching can get a direct view of complex process quickly. Based on the result analysis, the virtual Si etching goes following the rules we defined and the final finish figure is as illustrated in theory analysis. In addition, we use another method to simulate the etching process with adding more states and more ports, which can help to construct a more reasonable simulation structure, and the result is more close to the reality. In specific, we can realize the etching of plane <111> now, which is ignored in Assignment 2.

However, there are still some shortages:

1) Although we increase the model size, but the atom etching is in nanometer in practice, which is quite a large number and cannot be reflected fully in simulation;

2) We only simulate the rectangle, square and cross shape, anisotropy allows all kinds of pattern. So, we will continue to research the Cell_DEVS in etching with CD++ based on the current initial success.

3) When compare to the reality, the simulation here cannot control and adjust the etching velocity. In the following study, we will continue to research the effect of

etching velocity to the etching process and the final result.

4) Our simulation result is showed in 2D visualization, although it’s a 3D module. So, we will try to realize it in 3D visualization tool in the next step.

5. Reference

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