

PROCEEDINGS OF THE FIRST ANNUAL CONFERENCE ON COMPUTER-AIDED DEVELOPMENTS IN ELECTRONICS AND COMMUNICATION (CADEC-2019), VELLORE INSTITUTE OF TECHNOLOGY, AMARAVATI, INDIA, 2-3 MARCH 2019

# Computer-Aided Developments: Electronics and Communication

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## Foreword

On behalf of organising committee, we welcome you to the first annual conference on Computer-Aided Design in Electronics and Communication Engineering (CADEC 2019), held on date 2 – 3 March 2019. This is the first conference at VIT-AP University campus organized with the collective efforts of faculty members working in School of Electronics Engineering. We are very ambitious with this conference as in coming years we may plan to extend this conference at international level with indexing in web of conferences.

CADEC-2019 conference covers most of the major topics trending recent in Electrical/Electronics and Communication Engineering. The main focus of this conference is to cover major research breakthrough and updates in the Electrical/Electronics and Communication Engineering with broad perspective. Selecting high quality work through sufficient reviews was the top priority of this conference, so that collection of papers significantly aid to research and citation. We received around 65 contributions from India and abroad, out of which finally, 34 papers will be presented in two days sessions.

We are very grateful to Vice-Chancellor VIT-AP, Prof. D. Subhakar and Management VIT-AP, for their support to CADEC 2019; we extend our gratitude to advisory members for their support, and APPLY VOLT for their sponsorship. Also our gratefulness goes to keynote speakers: Prof. V. Rama Krishna Murthy, Dr. Siva Rama Krishna Vanjari, Er. Umesh Lohani, and Dr. Ravikumar Bhimasingu, who came to CADEC-2019 conference to share their work with the conference participants. We are confident that with strong presence of renowned faculty/industry peoples, the participants will benefit a lot and are advised to attend all the sessions.

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## A distinct carry select adder design approach for area and delay reduction using modified full adder

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**ABSTRACT:** A SQR Carry Select Adder (CSLA) design with modified full adder architecture is proposed in this work. The regular SQR CSLA has less delay but it is bulky when compared with other adders. The proposed design has reduced area and delay for a SQR CSLA. The architecture is designed for a 128bit and is synthesized, simulated in Vivado v2017.2 software. The result concludes that the new design is giving a considerable amount of reduction in area and delay. Also, the proposed design is of 128-bit therefore it can be used in the future designs of efficient processor.

**Keywords:** Carry select adder; Full adder; Linear CSLA multiplexer based full adder; SQR CSLA

### I. INTRODUCTION

In the digital signal processing (DSP) adders have higher precedence. Adders are the basic blocks of the digital signal processing chips and are of different types. The different types of digital adders includes ripple carry adder (RCA), carry skip adder (CSKA), carry look ahead adder (CLA), carry increment adder (CIA), carry save adder (CSA) and carry select adder (CSLA). Among all the digital adders CSLA has a higher speed [1]. In RCA the carry from the starting stage is rippled to the remaining stages. This increases the propagation delay and the output sum appears only when the carry reaches the particular stage. The delay in RCA is increased linearly with the size of the input bits.

The carry skip adder (also called as carry bypass adder) skips the carry at appropriate positions to boost the operation speed and the time required for this operation varies with respect to the data. The carry look ahead adder reduces the delay due to the propagation of the carry by looking at the lower adder bits of data and carry from the higher orders. The CLA design is more complex and it consumes more area when designed for more than 4-bits. In CIA, it is designed with RCA and an additional circuit that generates increment. Finally, in CSA the design has reduced delay by storing the carry generated in the present stage and by updating it on the next stage.

In all the adders propagation of carry and gate count in the propagation path are the major cause for delay. An efficient architecture that reduces the delay due to the

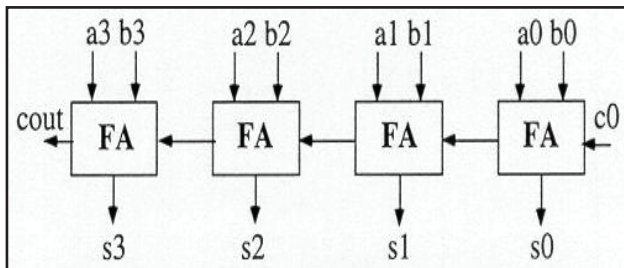
propagation of the carry is the CSLA. Bedrij proposed that the difficulty of carry transition delay is rectified by generation of multiple radix carries and simultaneously generated sums are selected by using these carries [2]. In CSLA the sum output is generated even before the carry from previous stages is generated. The structure of CSLA generates the sum output for  $C_{in} = 1$  and  $C_{in} = 0$  also and the multiplexer is provided with the output carry from the preceding stages. Regular CSLA has linear bit grouping unlike the SQRT CSLA which has non-linear bit grouping [3-7]. In CSLA the delay is reduced by pre-computing the output sum without the arrival of carry. The area consumed by the conventional CSLA is high compared with the other types of adders. The gate count and area are reduced by using a binary to excess-one code converter (BEC), the BEC is used to replace the RCA structure used for generating the sum output when carry from the previous stage is one [8-9]. To reduce the area consumption of CSLA further, the 1-bit full adders in the RCA are designed with multiplexers.

The multiplexer based full adder consumes less area when compared with the other conventional designs of the full adder because of only two transistors are required to implement a multiplexer. The proposed design has a full adder that is entirely designed using six multiplexers. The rest of the paper is organized as follows [section II](#) introduces the proposed architecture details. [Section III](#) elaborates the simulation results and comparisons. [Section IV](#) concludes the work.

## II. PROPOSED 128 BIT CSLA DESIGN:

The functioning of CSLA can be comprehended by analyzing it in three distinct stages. 1. Ripple carry adder, 2. Full Adders, and 3. Multiplexers.

A 4-bit RCA is shown in the [Figure 1](#). The RCA of 4bit is developed with 4 full adders (1-bit) connected in cascaded form. The RCA of K input bits is implemented with K full adder structures. An output of (K + 1) bits is generated from a K-bit RCA (K-bits for sum and an additional bit for carry). The existing design requires a more number of transistors than the proposed design [10]. The four full adders in [Figure 1](#) require, 8 EX-OR gates, 12 AND gates, and 8 OR gates. Since the implementation of the EX-OR gate requires a minimum of 12 transistors the area consumption is high when used excessively.



**Figure 1.** A 4-bit ripple carry adder using 4 full adders [2]

The multiplexers used in the CSLA design depends on the number of bits given to the RCA of the corresponding multiplexer. The sum output is chosen by the multiplexer between the responses of the RCA-1 and RCA-2 depending on the position of the  $C_{in}$ . When the  $C_{in} = 1$  RCA-2 output is chosen as the sum and when  $C_{in} = 0$  the response from the RCA-1 is considered by the multiplexer. The full adders used in the existing design are modified by the modified full adder structure. The modified full adder structure is given in Figure 3. It contains six 2:1 multiplexers for generating sum and carry. Since a multiplexer requires only 2 transistors, the area consumed by the designed adder is reduced by nearly 5% than the existing design. The comparison data can be viewed in TABLE 1. The full adder responses are the sum and carry, they are given in Boolean form as follows.

$$SUM = X_0 \oplus X_1 \oplus X_2 \dots\dots\dots (1)$$

$$CARRY = X_0.X_1 + X_1.X_2 + X_2.X_0 \dots\dots\dots (2)$$

From the Eq. (1) and (2) of SUM and CARRY, it is evident that SUM is generated by utilizing two 2-input EX-OR gates and CARRY is generated by utilizing three 2-input AND gates and two 2-input OR gates (or by one 3-input OR gate) [11]. The gate count is increased drastically when we use the normal full adder structure given in Figure 4. Especially the EX-OR will only require five other gates to implement. Since there is a number of full adders, the full adder is designated as the important block in the design of CSLA. So that area requirement is depended on the full adder design, for an efficient CSLA design the area consumed by the full adder should be as minimum as possible. For this reduction in area and power to be achieved the full adder can be designed using multiplexers only [12]. The multiplexer based designs have various implementations such as by using 4:1 multiplexers and some basic gates along with them. Also, the full adder can be designed by using 2:1 multiplexers and some basic gates along with them [13], [14]. Proposed design is efficient because it contains only multiplexers where routing is not complex, no other logic gates are used. This helps in the reduction of the delay to maximum extent.

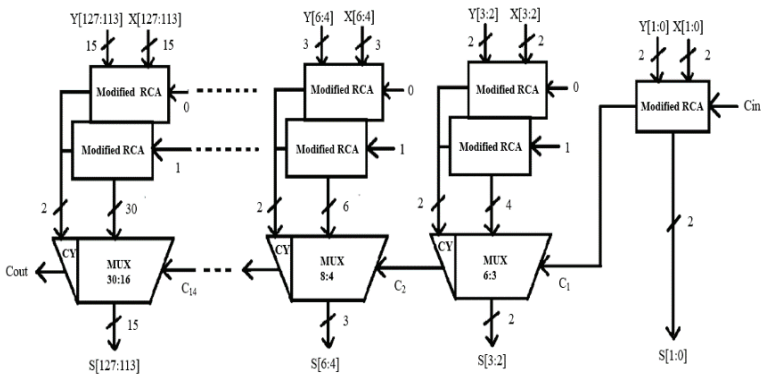


Figure 2. Proposed 128-bit CSLA design using modified full adder

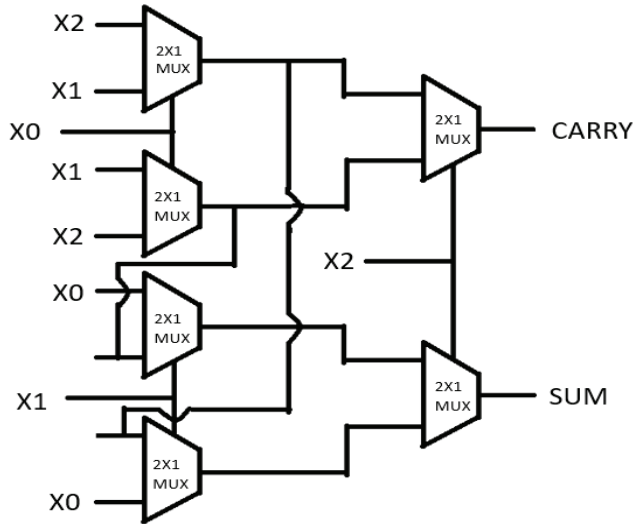


Figure 3. Full adder using six multiplexers [12]

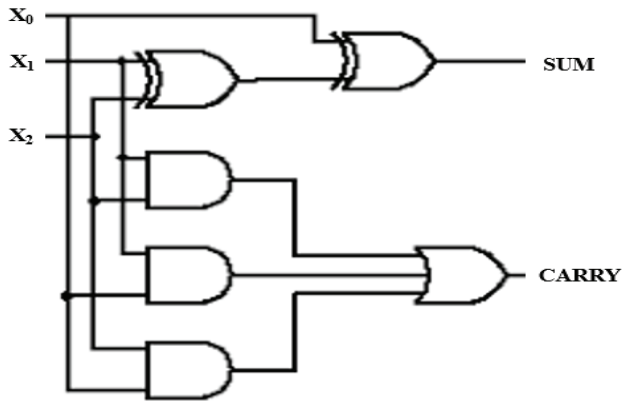


Figure 4. Basic full adder structure [12]

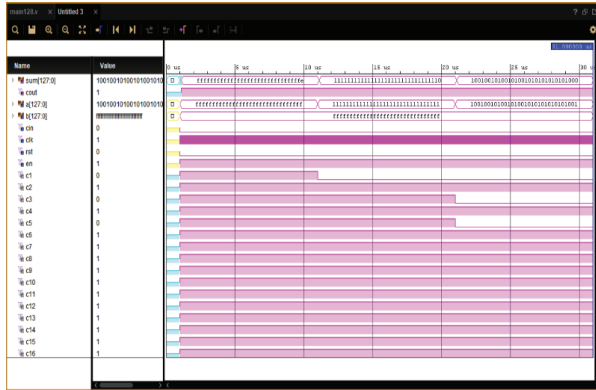
### III. RESULTS AND COMPARISONS

This proposed work is done in Verilog-HDL and simulated using the Xilinx Vivado 2017.2 software, the results of our modified full adder based design and the regular adder design are depicted in Figure 5 and Figure 6 respectively. The comparison of the area required by the regular 128-bit SQRT CSLA and our modified 128-bit SQRT CSLA is shown in Table I.

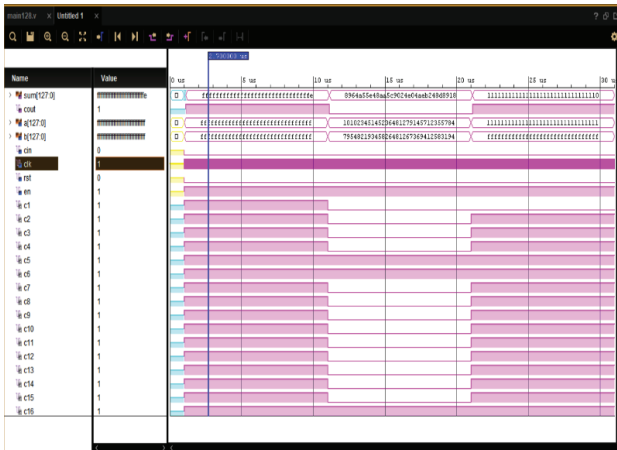


**Table I.** Comparison of area and delay of normal full adder based and modified full adder based structures

Adders name	Total number of LUTs consumed	Total delay	
		Setup	Hold
Normal full adder based SQR CSLA	270	5.984 ns	0.34 ns
Modified full adder based SQR CSLA	246	5.662 ns	0.34 ns

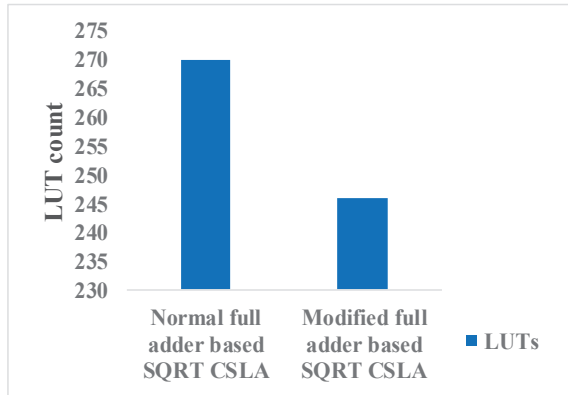


**Figure 5.** Results of the SQR CSLA with the modified full adder design

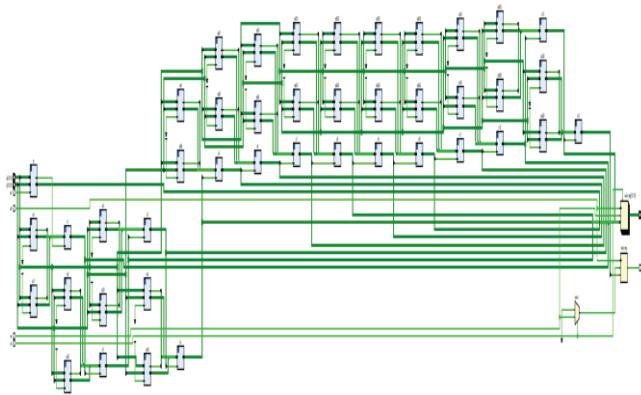


**Figure 6.** Results of 128-bit SQR CSLA with normal full adder design

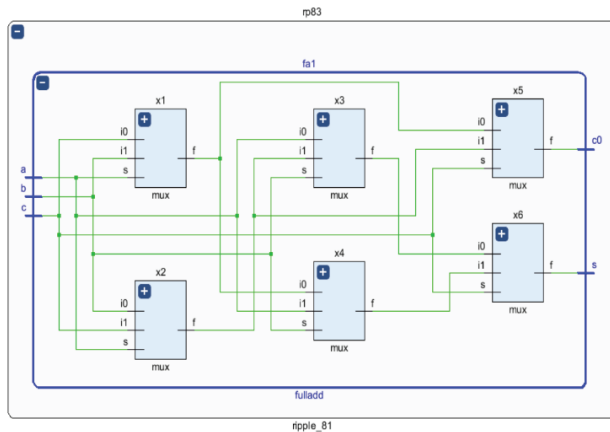
The comparison graph shown in [Figure 7](#) shows the difference in the area required. From the graphical analysis, it is evident that the area requirement of regular SQR CSLA is higher when correlated with our modified SQR CSLA. The RTL schematic of the proposed design is depicted in the [Figure 8](#). Individual ripple carry adder's RTL schematic is shown in [Figure 9](#). The delay results are shown in the [Table I](#). It is clear that there is an impressive reduction in delay for the proposed design when correlated with the regular SQR CSLA. The graphical analysis of delay is shown in the [Figure 10](#).



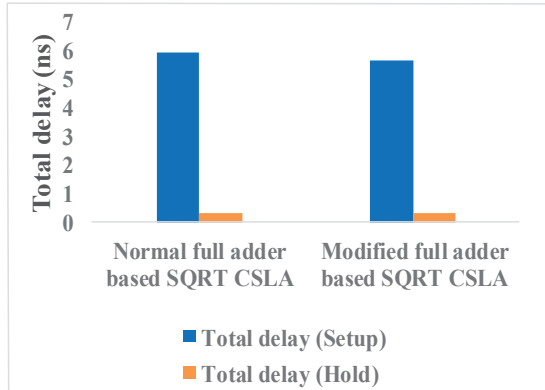
**Figure 7.** Plot showing the variation in consumption of LUTs for normal and modified structures



**Figure 8.** RTL schematic of modified full adder based Sqrt CSLA



**Figure 9.** RTL schematic of single block in the main architecture



**Figure 10.** Plot showing the variation in delay for normal and modified structures

#### IV. CONCLUSION

As the area and delay reduction are the critical issues of normal SQR CSLA. From the proposed design results, it is concluded that this can be reduced by the proposed design which consists of modified full adder replaced the normal full adder in the ripple carry adder block. The proposed design reduces the LUT count by 4.7% and the delay is reduced by 5.3%. In future work LUT count can be reduced by modifying the binary to excess-1 code converter in the CSLA structure.

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