Application of Hybrid System Theory to Switching Control of a Three-Phase Inverter

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Abstract- **A novel discrete event based current controller for three-phase load driven by power inverter is proposed. Main design specifications are robustness to load electrical parameters, fast dynamic response, reduced switching frequency and simple hardware implementation. To meet previous specifications a switching two types of controllers are developed: hysteresis type and Lyapunov type. The voltage source inverter (VSI) is represented as event driven system with 2^3 modes of operation. The switching among these modes is governed by the supervisory control approach.**

The overall stability of the system is shown using Lyapunov technique. The Lyapunov functions used contain a term penalizing incremental energy of control error, torque and stator currents, enhancing the stability. The regulation with the proposed control law provides good transient response of the brushless BLDC motor control. A new logical FPGA torque controller based on Lyapunov stability theory are developed, analyzed and experimentally verified.

I. INTRODUCTION

The power converter plays a fundamental role in a motor drives and its control strategy greatly influences the overall drive performance. Peak-to-peak current ripple, harmonic current contents, as well as acoustic noise depend directly on the control policy adopted for the inverter. Control of phase currents is very important issue too, since currents are directly related to the motor torque generation. Power amplifiers are usually VSI that can not directly impose load currents, a suitable feedback controller must be designed to this extent, [1].

Switching power converters are complex hybrid devices, which are becoming ubiquitous in many control applications. Since they usually operate at very high frequencies, their dynamic behavior is typically neglected in the controller design. However, the increasing demand on higher bandwidths and the stiffer constraints on harmonic generation make it necessary to incorporate their dynamics in modern control schemes, [2].

Power converters may be viewed as a set of voltage (or current) sourced subsystems interconnected through switches. The objective of the switches, which actuate as lossless transformers, is to allow the transfer of energy from one subsystem to another. The subsystems consist of passive elements (like inductors, capacitors, and resistances), power sources, and a load where the desired energy is delivered. Because of the presence of discontinuous elements the behavior of power converters consists of several modes, corresponding to different circuit topologies, i.e. two-level VSI presented in this paper with 2^3 modes, [3],[4].

However, significant research remains to be done in the direction of nonlinear control of systems that combine continuous and discrete events dynamics. To this end, we present a nonlinear control methodology for power electronic nonlinear systems, which captures the interaction of the underlying lower-level continuous dynamics with the upper-level discrete or logical components of digital controller. Initially, we cast these systems as variable structure multi-modal systems in which each mode is governed by continuous dynamics, whereas the transitions between the modes are controlled by discrete events. Then, using multiple Lyapunov functions [5], one for each continuous mode, we synthesize a family of bounded nonlinear controllers that enforce the desired stability and performance properties within each individual dynamical mode in the presence of input constraints. The controller synthesis procedure yields also an explicit characterization of the stability region associated with each mode. Finally, we derive a set of switching rules that orchestrates the transition between the constituent modes and their respective controllers, in a way that ensures asymptotic stability and reference-input tracking in the overall constrained switched closed-loop system, [6]. The proposed methodology is successfully applied to a novel means of designing and effective torque and speed control for BLDC, [7].

After a general introduction, system analysis is performed, control targets are specified, and the proposed control strategy is presented and discussed. Further, FPGA based controller architecture is shown and experimental results are presented using a BLDC motor as the inverter load. However, this does not limit the wider applicability of the proposed controller that is suitable for different types of three-phase AC loads.

II. HYBRID SYSTEM FOCUS

Hybrid systems can be viewed as a large collection of systems of various classes. A hierarchical structure arises when a logical control unit governs such a system by issuing logic decisions. This leads to the system framework shown below in figure which clearly illustrates this architecture (Fig. 1), [8].

The top layer, which is a discrete event system, can use different types of description language such as finite state

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machines, fuzzy logic, Petri nets, etc. The bottom layer is a continuous system, and is usually the physical system. The interface plays the role of facilitating communication between the two different layers by means of translating signals between them. As the techniques for control design and analysis are well developed for the continuous and discrete systems, the design of the interface is of utmost importance because it determines the way in which the combined system behaves. This control architecture which has just been described appears in a wide variety of applications and forms the heart of most hybrid system designs. For most system designs, the logic unit and continuous unit are usually designed separately and then combined together by an interface, [9]. Another approach is converting the whole system to be purely logic or continuous for design. As you may realize, the modeling of a hybrid system is not an easy job, [10].

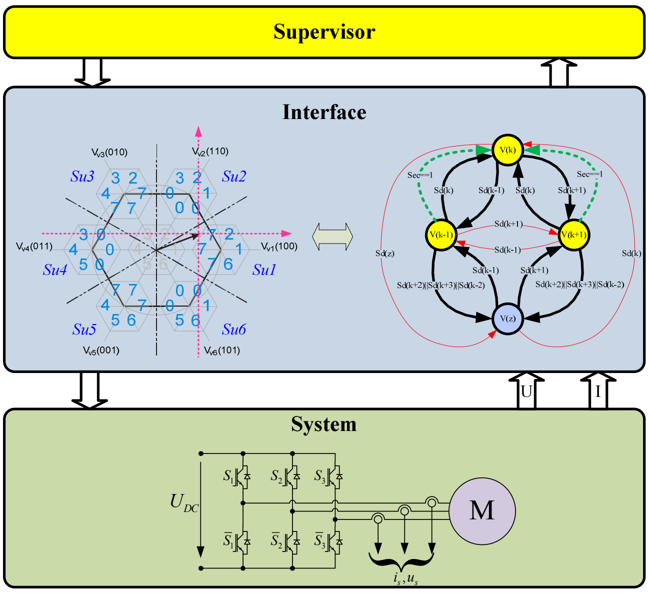


Fig. 1. Hybrid control architecture.

The control problem is formatted backwards starting from the BLDC motor. First, we use the torque as reference input. After the reference torque is given, the motor needs a certain amount of current in order to provide the desired torque. The VSI inverter serves as motor controller to request this current i_s^d from the output of speed controller.

III. SYSTEM ANALYSIS AND CONTROL

The basic circuit of a VSI feeding a Y-connected three-phase load is presented in Fig. 2, where the load has been modeled by phase resistance, inductance and induced voltages. The voltage and the phase currents equations of the Y-connected three-phase load are:

$$u_{sk}(S_i) = R_s\, i_{sk} + L_s \frac{d\, i_{sk}}{dt} + e_{sk}; \quad k = 1,2,3, \quad i = 0,1,\ldots,7\,, \tag{1}$$

$$i_1 + i_2 + i_3 = 0\,. \tag{2}$$

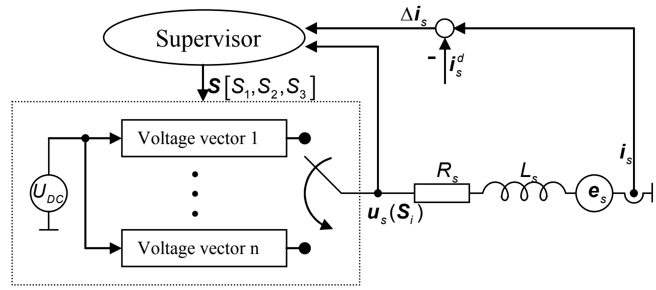


Fig. 2. Block diagram of DES current control.

The considered control problem is the tracking of a three-phase current reference signal. After the current control error is defined $\Delta \boldsymbol{i}_s = \boldsymbol{i}_s - \boldsymbol{i}_s^d$, rewritten in error form becomes

$$L_s \frac{d}{dt}\Delta \boldsymbol{i}_s + R_s\, \Delta \boldsymbol{i}_s = \boldsymbol{u}_s(\boldsymbol{S}_i) - \boldsymbol{e}_s\,, \tag{3}$$

which contains all the disturbances (exogenous and endogenous) action on the system.

The hybrid control architecture consists of a family of discontinuous input functions and a supervisor; at each instant, the supervisor selects a particular input function from the family. The supervisor controls the input function selection via particular voltage vector Si as well as when the selection changes. Such hybrid controllers have often been called logic-based switching controllers and are the most widely studied class of hybrid controllers, [11]. The supervisor selects a input function to be active by specification of control Lyapunov function.

Consider the error model as given by (3), the method proceeds to solve for the feedback control $\boldsymbol{u}_s(\boldsymbol{S}_i)$. The feedback controller is referred as the equivalent control [6]

$$\boldsymbol{u}_{sequ} = \boldsymbol{e}_s - R_s\, \boldsymbol{i}_s - L_s \frac{d\, \boldsymbol{i}_s^d}{dt} \tag{4}$$

The controller so obtained represents virtual feedback control action that, in the absence of perturbations and modeling errors, ideally keeps the system responses evolving on manifold represented by the condition $d\left(\Delta \boldsymbol{i}_s\right)/dt = 0$, [12].

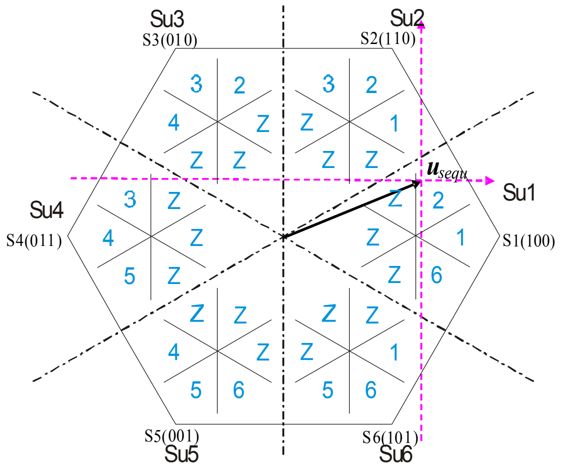
Let us propose Lyapunov function $V = \Delta \boldsymbol{i}_s^{\,T} \Delta \boldsymbol{i}_s / 2$. Its time derivative along the trajectories can be expressed in terms of $\boldsymbol{u}_{eq}$ as

$$\dot{V}_i = \Delta \boldsymbol{i}_s^{\,T} \Delta \dot{\boldsymbol{i}}_s = \Delta \boldsymbol{i}_s^{\,T} \left(\boldsymbol{u}_s(\boldsymbol{S}_i) - \boldsymbol{u}_{sequ}\right)/L_s < 0, \quad i = 0,1,2,\ldots,7\,. \tag{5}$$

So now the problem is translated into the selection of a vector $\boldsymbol{u}_s(\boldsymbol{S}_i) \in U\left[\boldsymbol{S}_0, \boldsymbol{S}_1, \boldsymbol{S}_2, \boldsymbol{S}_3, \boldsymbol{S}_4, \boldsymbol{S}_5, \boldsymbol{S}_6, \boldsymbol{S}_7\right]$ in such a way that $\dot{V}$ is always negative definite.

The switch positions of the three-phase inverter are described using the logical variables $\boldsymbol{S}_i$, dependent if switch S_i is ON or OFF. Each variable corresponds to one phase of the inverter (Fig. 1). Three-phase inverter can produce 2^3 voltage vector combinations; two of them are zero vectors and 6 active vectors, Fig. 3.

The energy flow between the input and output side of the three-phase inverter is controlled by switching matrix. By introducing the binary variables S_i that are "1" if particular switch S_i is On and "0" if switch S_i is OFF (i=1,2,3,…,6) the behavior of the VSI switching matrix can be described by the three dimensional vector $\boldsymbol{u}_s = U_{DC}\, \boldsymbol{L}\, \boldsymbol{S}_i$, where matrix $\boldsymbol{L}$ and vector $\boldsymbol{S}(S_1, S_2, S_3)$ are defined as [13]:



$$SZ(k) = \begin{cases} S0; S(k-1) = S0 \vee S1 \vee S3 \vee S5 \\ S7; S(k-1) = S7 \vee S2 \vee S4 \vee S6 \end{cases}$$

Fig. 3. Stator voltage $\boldsymbol{u}_s(\boldsymbol{S}_i)$ of three phase inverter.

$$\boldsymbol{L} = \begin{bmatrix} 1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \end{bmatrix} . \tag{6}$$

$$\boldsymbol{S}^T = \begin{bmatrix} S_1 & S_2 & S_3 & \bar{S}_1 & \bar{S}_2 & \bar{S}_3 \end{bmatrix}$$

Relation (6) is true for the two-level inverter circuits. It essentially shows that this particular switching matrix is able to generate three independent control actions denoted as the components S_1, S_2 and S_3 of the control vector

$$\boldsymbol{u}_s(\boldsymbol{S}_i) = U_{DC}\left[S_1 + S_2 e^{j2\pi/2} + S_3 e^{-j2\pi/3}\right]. \tag{7}$$

In the proposed new developed switching voltage space vector modulator voltage vectors $\boldsymbol{S}_i$ can be mapped into the three-phase plane as shown above in Fig. 3. This provides a geometric interpretation of the voltages that can be produced by the inverter.

IV. Switching Strategy

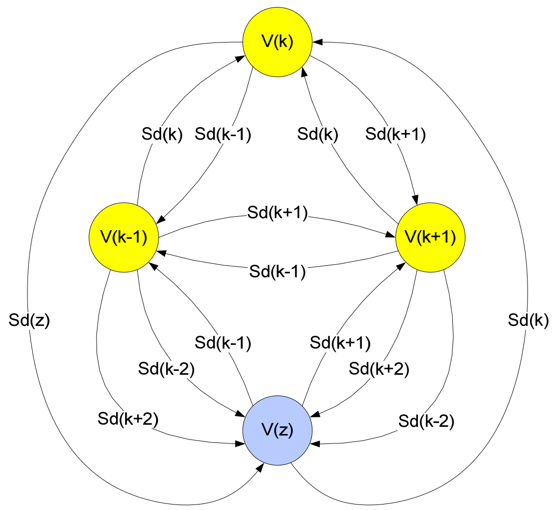
A. Hysteresis based Switching Control

To consider a hysteresis controller as a discrete-event dynamical system, it allows focusing in much more details on the switching actions and will enable a better understanding of the controller design. A DES system reacts only if an event is recognized. To control the current $\boldsymbol{i}_s$, the sector of drive voltage $\boldsymbol{u}_{sequ}$ is recognize first, and based on the known sector, the input voltage vector $\boldsymbol{u}_{si}(\boldsymbol{V}_k)$ (the transistor switching pattern) for the current control is selected, respecting the current control error $\Delta \boldsymbol{i}_{si}$ (3)

Considering space vector representation of the stator voltage $\boldsymbol{u}_s(\boldsymbol{V}_k)$ (7), the voltage is represented as vector rotating around the origin. Six active switching vectors of the three-phase transistor inverter represent the six active output voltage vectors denoted as $\boldsymbol{V}_1 ... \boldsymbol{V}_6$; $\boldsymbol{V}_0$ and $\boldsymbol{V}_7$ are two zero voltage vectors. According to signs of the phase voltages u_{s1}, u_{s2} and u_{s3}, the phase plane is divided into six sectors denoted by Su1 … Su6, Fig. 3.

In regards to the situation (Fig. 3), the stator voltage space vector $\boldsymbol{u}_{sequ}$ is in sector Su1. In this sector, logical voltage vectors $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_6$ and $\boldsymbol{V}_7$ are selected for the current control. $\boldsymbol{V}_0$, $\boldsymbol{V}_7$ are two zero vectors, while $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_6$ are three nearest adjacent live output voltage vectors to this sector. With the use of the DES theory, five output voltage vectors $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_6$ and $\boldsymbol{V}_7$ are recognized as discrete states of the system. Events represent allowed transition among the discrete states i.e. allowed switching and are determined via stability issue.

A FSM on Fig. 4 presents a state transition diagram of DES controller. The states $\boldsymbol{V}(k)$ represent the input voltage vector $\boldsymbol{u}_{si}(\boldsymbol{V}_k)$ of three-phase inverter in Fig. 3, for each voltage sector of BLDC motor voltage $\boldsymbol{u}_{si}$. $\boldsymbol{V}(k)$ represents active voltage vector and $\boldsymbol{V}(z)$ produced zero voltage vectors of VSI inverter.



$$k = 1,2,3,4,5,6$$

$$z = \begin{cases} 7; k = 1,3,5 \\ 0; k = 2,4,6 \end{cases}$$

Fig. 4. State transition diagram.

The proposed logical event-driven BLDC current control can be realized in the form described in Table I, where states of current control error are presented by *sign*($\Delta \boldsymbol{i}_s$) and currently active voltage sector is presented by *sign*($\boldsymbol{u}_s$).

To further improve the presentation, active voltage vectors are marked in Table I with a blue background. Because the transition between inverter switch states is performed by switching only one inverter leg, switching frequency and current chattering (and consequently torque chattering of BLDC motor) are reduced.

The driving signal of inverter switches can be generated with FPGA circuit. The considered control task is a tracking of three-phase current reference signal. The zero voltage control vector can be consciously used to reduce the transistor's switching frequency.

TABLE I
I. LOOK-UP TABLE.

sign($\boldsymbol{u}_s$) / sign($\Delta\boldsymbol{i}_s$)		Su1	Su2	Su3	Su4	Su5	Su6
		100	110	010	011	001	101
Sdi0	000	VZ	VZ	VZ	VZ	VZ	VZ
Sdi1	100	V1	V1	VZ	VZ	VZ	V1
Sdi2	110	V2	V2	V2	VZ	VZ	VZ
Sdi3	010	VZ	V3	V3	V3	VZ	VZ
Sdi4	011	VZ	VZ	V4	V4	V4	VZ
Sdi5	001	VZ	VZ	VZ	V5	V5	V5
Sdi6	101	V6	VZ	VZ	VZ	V6	V6
Sdi7	111	VZ	VZ	VZ	VZ	VZ	VZ
	$\mathrm{VZ(k)} = \begin{cases} \mathrm{V0;\ V(k\text{-}1)=V0 \vee V1 \vee V3 \vee V5} \\ \mathrm{V7;\ V(k\text{-}1)=V7 \vee V2 \vee V4 \vee V6} \end{cases}$						

B. Lyapunov based Switching Control

Hysteresis bang-bang approach is a fast and robust control, namely used for simple converter systems. Taking into consideration that such controllers may be presented as discrete event systems, it opens a more systematic view and enables controller design. In order to ensure convergence or stability, there are very valuable Lyapunov function based approaches for the design of the global stability of closed loop control.

In order to improve the transient response of the control system, and to try to reduce the control effort and current ripple, we propose the selection of control input $\boldsymbol{u}_s(\boldsymbol{S}_1, \boldsymbol{S}_2, \boldsymbol{S}_3, \boldsymbol{S}_4, \boldsymbol{S}_5, \boldsymbol{S}_6, \boldsymbol{S}_7)$ based on control Lyapunov function (CLF), [13].

The task of the controller is to switch among combinations of switches, depending on the encountered event-switching state, in order to compensate the energy dissipation. Just as the existence of a Lyapunov function is necessary and sufficient for the stability of a system without inputs, the existence of a control Lyapunov function is necessary and sufficient for the stabilizability of a system with a control input, [15].

The CLF paradigm is extremely powerful. It suggests the search for stabilizing switching vector inputs $\boldsymbol{u}_s(\boldsymbol{S}_i)$ in (5) by interactively solving a static nonlinear programming problem: when at state $\boldsymbol{i}_s(t_i)$ find such $\boldsymbol{u}_s(\boldsymbol{S}_i)$, that (5) holds. Closed-loop inverter current control (3) will be stabilized by using state feedback controller if and only if system admits a CLF.

The use of CLF approach, which can be used in order to decrease the number of inverter switching, consists of keeping the same value of switching vector $\boldsymbol{S}_i$ until the trajectory of (5) hits the switching surface defined by $\dot{V}_i = 0, i = 1,2,3,\ldots,7$ and to choose on that surface a new value of switching vector $\boldsymbol{S}_{i+1}$ or $\boldsymbol{S}_{i-1}$ such that again will be $\dot{V}_{i+1} < 0$. How much times the system spend at particular state *i* is expressed as a difference of the timed sequence of events $\Delta t_i = t_{i+1} - t_i$, i.e. duty cycle $d_i = \Delta t_i$.

V. IMPLEMENTATION

The proposed approach is based on fast parallel processing and suitable for a Field Programmable Gate Array (FPGA) implementation. In such implementation it would be possible to reproduce near ideal switching mode process. However, with FPGA implementation, designer has a difficult task to characterize and describe the hardware architecture that corresponds to the chosen control algorithm. FPGA designers must follow an efficient design methodology in order to benefit from the advantages of the FPGAs and their powerful CAD tools. From software point of view, HDL modeling system is based on using the variables that request logic values, too, [16].

Fig. 5 presents the general structure of the different elementary modules. As shown in Fig. 5, Xilinx Spartan XC3S1200E is used to implement the BLDC motor controller. This motor control Intellectual Property (IP) is divided into three parts. The first part is the driver's part with ADC and DAC management modules, incremental module for speed and position measurement and RS 232 module for connection of host PC equipment with Matlab/Simulink program environment. The second part includes the PI-speed motor controller. Output of speed controller is a measure for the desired torque of BLDC motor that multiplies the three-phase reference currents of machine. The currents phases are depend on rotor position. The third part includes the look-up table with hysteresis current controller and an average output voltage of BLDC motor synchronization – voltage sector selection, Fig. 5.

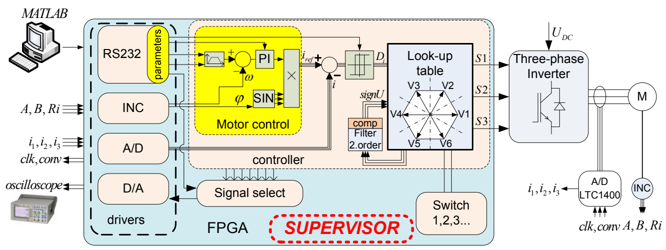


Fig. 5. FPGA controller of the BLDC motor.

The FPGA based BLDC system (Fig. 5) is meant to be operated according to certain established rules and principles, which are presented as infinite state machine (ISM). Fig. 6 shows on the left hand side normal machine operation including start/shut/up/down operation. The ISM on the right hand side represents a potential risk for the BLDC with inverter if a major drive parameters drifts into it, or if a failure occurs.

A low cost Xilinx Spartan 3 FPGA that contains 1.2 M logical gates and includes a 50 MHz oscillator was used as a target component for the implementation of the controller. The architecture of each control algorithm is designed according to an efficient methodology that offers considerable design advantages such as reusability, reduction of development time and optimization of the consumed resources. Each control algorithm is portioned into elementary modules, which are easier to develop and are more functional, [17].

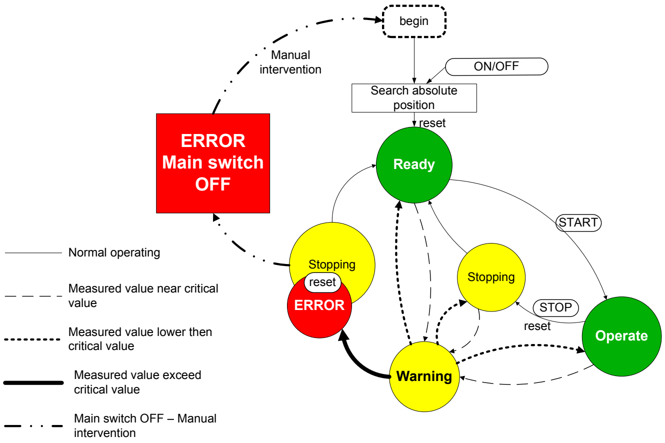


Fig. 6. State CAD diagram.

Such a scheme for operation occupied 35% of the “number of 4 input LUTs” FPGA circuit and 67% of 18-bits multipliers.

VHDL code was created in Xilinx ISE software. Software scheme is divided into individual blocks for better review. It is composed of a data path and a control unit coded in VHDL. The data path is composed of a fain gain operators such as adders, multipliers, multiplexers and registers. The data transfer between these operators is managed by a control unit, which is synchronized with the clock signal (CLK). The control unit of the developed modules is always activated via Start pulse signal. When the computation time process is over, an End pulse signal indicates that the data outputs of the module are ready.

VI. RESULTS

The simulation results with hybrid based speed and current BLDC control are presented next. The results of the start-up characteristic under change of load and reference is shown on Fig. 7 – motor currents, reference torque, estimated machine torque, load torque and estimated rotor speed.

In order to test the proposed Xiling SPARTAN 3A FPGA-based controller, experiments were carried out on in-house built FPGA prototyping platform. In all simulation and experimental results, the BLDC motor from Maxon, type EC32 with parameters $R_s = 0{,}56\ \Omega$, $L_s = 0.09$ mH, $J = 20$ gcm^2, $\Psi_{PM} = 0.0205$ Vs, $t_M = 6.6$ ms was used.

The FPGA controller has the diagnostic features that are necessary for drive installation, test problem detection and elimination. The control algorithm is executed every 2.5 μs, and the switching frequency of three-phase inverter was set with the tolerance band of the hysteresis current control. The control of both, the speed and applied torque, is possible, thus hardware in the loop operation can also be performed.

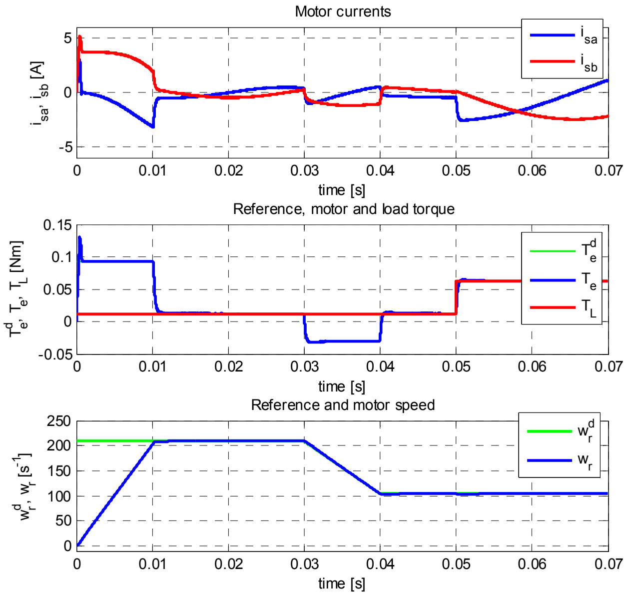


Fig.7. Motor currents i_{sa}, i_{sb}, reference motor torque T_e^d, motor torque T_e, load torque T_L, reference ω_r^d and actual rotor speed ω_r.

The experimental results are illustrated in Fig. 8 and Fig. 9. The results are recorded with an oscilloscope and consequently the measured results are contaminated with noise.

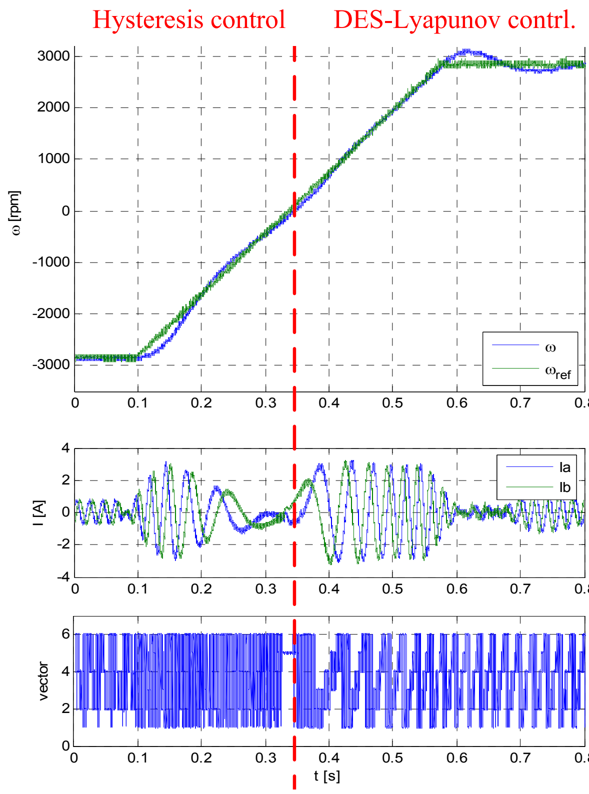


Fig. 8. Active voltage vectors and currents at progressive change of reference speed.

Fig. 8 shows the transient of speed (ω) currents (i_a, i_b) and voltage vectors (spectrum) $V_i(S_1, S_2, S_3)$ of three-phase inverter. Starting with hysteresis controller and at change speed sign is switched to the proposed hybrid DES-Lyapunov controller.

DES control successfully reduces the numbers of switching. Fig. 9 (b) shows the numbers of switching at a constant motor's speed of 2000 rpm within the interval of 1 ms. The difference between the hysteresis and DES-Lyapunov control is the highest at low velocities. With increasing speed this difference decreases. However, reducing of switching frequency, increases current waving.

VII. Conclusion

The idea of hybrid-based control of event-driven systems is used for the design of event-driven current controller and auxiliary steering and protection functions for a three phase inverter. Individual control functions have been designed, using the proposed approach, and integrated into the overall functionality description of the inverter. Overall functionality of the inverter and the performance of the proposed event driven current control were checked by simulations and experimentally confirmed. Special attention is paid to the mapping of the proposed design approach into the schematic form for the FPGA implementation.

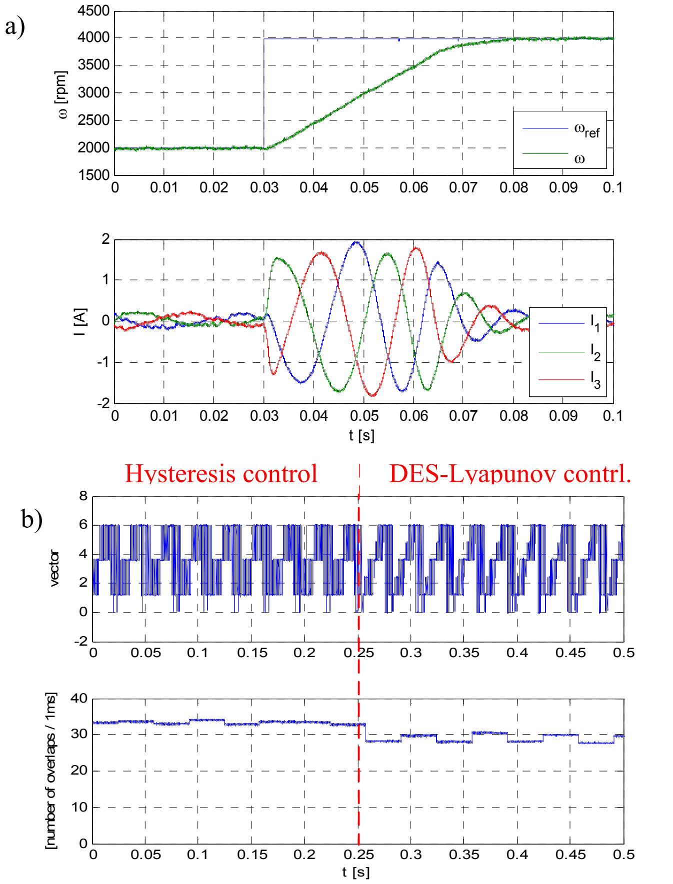


Fig. 9. Experimental results: (a) Step response and (b) switches number of switching elements at 2000 rpm.

The simulation and experiments confirmed potential of the presented approach: traditional coding efforts are significantly reduced on one hand, and on the other hand the control algorithm can be verified off-line. Formal mathematical background of the proposed approach and its correspondence to the conventional control system theory opens further possibilities for the design, simulation, and formal analysis of the discrete event systems. The proposed approach offers a promising technique for design of complex and timely critical algorithms. On one hand, future research is oriented towards the optimization of the introduced current control strategies, and on the other hand towards the formalization of analysis and control design methods.

References

[1] I. Boldea, and N.L. Tutelea, *Electric machines: steady state, transients, and design with Matlab*. CRC Press, Taylor and Francis Group, 2009.

[2] G.S. Buja, and M.P. Kazmierkowski, "Direct torque control of PWM inverter-fed AC motors – A survey". *IEEE Trans. Ind. Electronics*, vol. 54, no. 4, pp. 1824-1842, 2004.

[3] J. Buisson, P.Y. Richard, and H. Cormerais, "On the stabilization of switching electrical power converters". In *Hybrid Systems: Computation and Control*, pp. 184-197. Springer, Berlin / Heidelberg, 2005.

[4] M. Senesky, S.M. Eirea, and T.J. Koo, "Hybrid modelling and control of power electronics". In O. Maler, and A. Pnueli (ed.), *Hybrid Systems: Computation and Control, (Lecture notes in computer science)*, pp. 450-465, Springer, Berlin / Heidelberg, 2003.

[5] M.S. Branicky, "Introduction to hybrid systems". In D. Hristu-Varsakelis, and W.S. Levine (ed.), *Handbook of Networked and Embedded Control Systems*, pp. 91-116. Boston: Birkhauser, 2005.

[6] V.I. Utkin, *Sliding Modes in Control and Optimization*. Springer Verlag. Berlin, 1992.

[7] K. Jezernik, R. Horvat, and M. Čurkovič, "Nonlinear torque control of BLAC motor". In Proc. 2010 IFAC Symposium on Mechatronics Systems, Cambridge, USA, pp. 453-460, 2010.

[8] X.D. Koutsoukos, P.J. Antsaklis, J.A. Stiver, and M.D.Lemmon, "Supervisory control of hybrid systems". *Proceedings of the IEEE*, vol.88, no. 7, pp. 1026-1049, 2000.

[9] C.G. Cassandras, and S. Lafortune, *Introduction to Discrete Event Systems*. 2nd ed. Springer Science + Business Media, 2008.

[10] G.A. Wainer, *Discrete-Event Modeling and Simulation: A Practitioner's Approach*. CRC Press, Taylor and Francis Group. Boca Raton, 2009.

[11] D. Liberzon, "Switched systems". In D. Hristu-Varsakelis, and H.S. Levine (ed.), *Handbook of Networked and Embedded Control Systems*. pp 559-574, Boston: Birkhauser, 2005.

[12] V.I. Utkin, V.I., "Sliding mode control design principles and applications to electric drives". *IEEE Trans. Ind. Electron*., vol. 40, no.1, pp. 23-36, 1993.

[13] A. Šabanović, K. Jezernik, and N. Šabanović, "Sliding modes applications in power electronics and electrical drives". In X. Yu, and J.X. Xu (ed.), *Variable structure systems: Towards the 21st century, (Lecture notes in control and information sciences)*. pp. 223-251, Springer, Berlin / Heidelberg, 2002.

[14] A. Polič, and K. Jezernik, "Event-driven current control structure for a three phase inverter". *Int. rev. electrical eng. (Testo stamp.)*, vol. 2, no. 1, pp. 28-35, 2007.

[15] Z. Artstein, "Stabilization with relaxed control". *Nonl. Anal.*, TMA vol. 7, pp. 1163-1173, 1983.

[16] E. Monmasson, and M.N. Cirstea, "FPGA Design Methodology for Industrial Control Systems – A Review". *IEEE Trans. Ind. Electronics*, vol. 54, no. 4, pp. 1824-1842, 2007.

[17] B. Bomar, "Implementation of a micro programmed control in FPGA". *IEEE Trans. Ind. Electronics*, vol. 49, no. 2, pp. 415-422, 2002.