Published in IET Power Electronics
Received on 2nd April 2010
Revised on 18th November 2010
doi: 10.1049/iet-pel.2010.0275

ISSN 1755-4535

Implementation of discrete event control for brushless AC motor

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Abstract: This study presents the implementation of a hybrid control strategy that is applied to a brushless AC (BLAC) motor drive. Hybrid control is a general approach for control of switching-based hybrid systems (HS). This class of HS includes a continuous process, controlled by a discrete controller with a finite number of states. The overall stability of the system is shown with the use of Lyapunov technique. The Lyapunov functions contain a term that penalises incremental energy of control error, torque and stator current, which enhances the stability. The closed-loop system, with the proposed control law, provides good transient response and good regulation of the BLAC motor control. A new logical field programmable gate array current (torque) controller is developed, based on the Lyapunov theory. The reference tracking performance of speed and torque (current) is demonstrated in terms of transient characteristics through simulation and experimental results.

1 Introduction

The non-linear and complex dynamic interactions of an AC machine, because of many parameters that cannot be measured, are causing considerable difficulties in motor management. Additionally, the uncertainties that come up from lack of knowledge of system inputs and inaccuracies in the mathematical modelling itself, contribute to performance degradation of the feedback control system. Over the years, it has been generally accepted that the orientation field, in one of its many forms, is the most promising control method for a high dynamic performance AC drive [1].

The brushless AC (BLAC) motor is now widely used in industrial drive application because of its many advantages, such as high power factor, high torque density, high efficiency, small size and weight. A position sensor is required to enable high quality control and performance of a BLAC motor, which increases the overall cost of a drive system. This paper introduces recently developed hybrid-based approach for modelling of discrete event systems in the field of power electronics and motion control. Power electronic circuits are hybrid dynamic systems. Because of the ON and OFF switching of power electronic devices, the operation of power electronic circuits can be described by a set of discrete states with associated continuous dynamics. A hybrid structure arises when a logical control unit governs such a system by using a logic decision [2].

Controller's implementation on field programmable gate array (FPGA) is a good solution for logical operations. Output condition of logical gates depends on inputs, and there is no additional time cycle delay. Logic gates connection on FPGA allows all processes to be executed in parallel. Comparison of FPGA system with the digital signal processor (DSP) shows that because of the parallel architecture of processes, FPGA system is faster and more appropriate for processes with logical decisions and mathematical operations. Short response time of FPGA system is very beneficial in supervising. Supervisor can be implemented simultaneously and it can affect the operation at any time, while in the DSP it is necessary to wait for next time cycle to change the decision. In more complex systems, the cycle time could be also 50 μs. However, the most important advantage of DSP systems is that they are widespread technology and frequently used in similar application. These are the most important advantages between the DSP and FPGA.

In this paper, a hybrid control law, based on Lyapunov stability theory, without linearisation, is proposed which strictly quarantines a sufficient stability region in the state space for the system against large-signal disturbances. In this approach, Lyapunov direct method is used, which is the most important tool for non-linear control system design [3].

In using the direct method, the idea is to construct a scalar-energy-like function (Lyapunov function) for the system and to examine the function's time variation. The closed-loop system with the proposed control law does not only guarantee a sufficient stability region, but also provides a good transient response and good regulation.

The aim of this paper is to design a control law for BLAC motor to achieve a good torque control in a steady-state and transient operating conditions. The feedback system is globally asymptotically stable in the means of the Lyapunov stability theory. Therefore we are interested in the extension of the Lyapunov function concept. This concept uses a scalar function that contains a logical discontinuous input switching function that penalises the torque, that is, current control error and enhancing the stability.

2 BLAC motor control

The BLAC motor combines many of the advantages of the permanent excited AC motor and the synchronous motor [4]. The BLAC motor needs low reactive current, which is very similar to the DC motor, and the current is proportional to the torque. The shaft torque is therefore easy to estimate by detecting a three-phase current of BLAC motor. The BLAC motor is the combination of a permanent excited synchronous motor and a three-phase inverter. The BLAC motor dynamics are governed as electrical current with

$$\frac{\mathrm{d}i_{sk}}{\mathrm{d}t} = \frac{1}{L_s}(u_k - R_s\, i_{sk} - e_{sk}); \quad k = 1, 2, 3 \tag{1}$$

where i_{sk} denotes three-phase stator currents, u_{sk} phase voltage and e_{sk} electromagnetic force voltage. Developed torque of BLAC motor is

$$T_{\mathrm{e}} = \frac{\Sigma_{k=1}^{3} e_{sk} i_{sk}}{\omega} \tag{2}$$

The mechanical equation is

$$\frac{\mathrm{d}\omega}{\mathrm{d}t} = \frac{1}{J}(T_{\mathrm{e}} - T_{\mathrm{L}}) \tag{3}$$

where ω is shaft speed, T_{e} and T_{L} are electromechanical and load torque, respectively.

The commutation of BLAC motor depends on the position of the rotor. The angle between the magneto motive forces of the stator and the rotor is fixed to 90°, so the motor produces maximum torque and needs low reactive current.

In our model (Fig. 1) current component i_d and i_q are not measured directly. Like in the classical field-oriented control (d–q model), d-axis is set to zero (provided that correct rotor position is known), therefore the q-axis current component i_q is equivalent with the amplitude of the reference current (Fig. 1).

We have performed a simple speed control of BLAC motor. Fig. 1 shows the architecture of speed/current regulation of BLAC motor implemented onto a FPGA circuit. The considered control task tracks a three-phase current reference signal, whose amplitude is determined by the output of proportional–integral (PI) speed controller. Drivers are made to incorporate every external device. A 'signal select' output is implemented onto FPGA for monitoring and external supervisor activity [5].

3 Hybrid system focus

Historically, the most common class of control architectures has been based on linear feedback. In the case of classical non-linear controllers, there has been substantial growth in recent years in control design methods that are based on feedback linearisation, passivity, adaptation and control Lyapunov functions.

Hybrid controllers can be used to obtain improved closed-loop performance, beyond what can be achieved with the use of either classical linear or smooth non-linear controllers. Motivation for use of hybrid control is that the performance of a hybrid closed loop can exceed the performance that can be achieved by any fixed feedback controller without switching. The results that we subsequently present illustrate the realisation of this potential [6].

Hybrid controllers are represented by the block diagram in Fig. 2, that is, the hybrid control architecture consists of a family of non-linear feedback functions and a supervisor. At each instant, the supervisor selects a particular feedback function from the family and then it controls the feedback function selection via particular voltage vector $u_s(V_i)$, $i = 0, 1, 2, \ldots, 7$ as well as when the selection changes. Such hybrid controllers have often been called logic-based switching controllers and are the most widely studied class of hybrid controllers [7] (Table 1).

The supervisor selects a feedback function to be active by specification of control Lyapunov function. The supervisor, as well as the family of feedback functions, may include dynamics and delays or other memory elements. The supervisor can be time-driven, in which case the switching is the time set as in a digital controller; or it can be event-driven [8], in which case the switching occurs according to a state partition or a state-dependent switching condition. For the supervisor, this structure allows transitions between feedback function selections according to an automata model and the common hybrid control architecture. It is important that the supervisor does not switch between feedbacks functions infinitely often in a finite time period which can be achieved in a number of ways. Design of the complete hybrid controller involves specification of both the family of feedback functions and specification of the switching logic. There is little guidance in the published

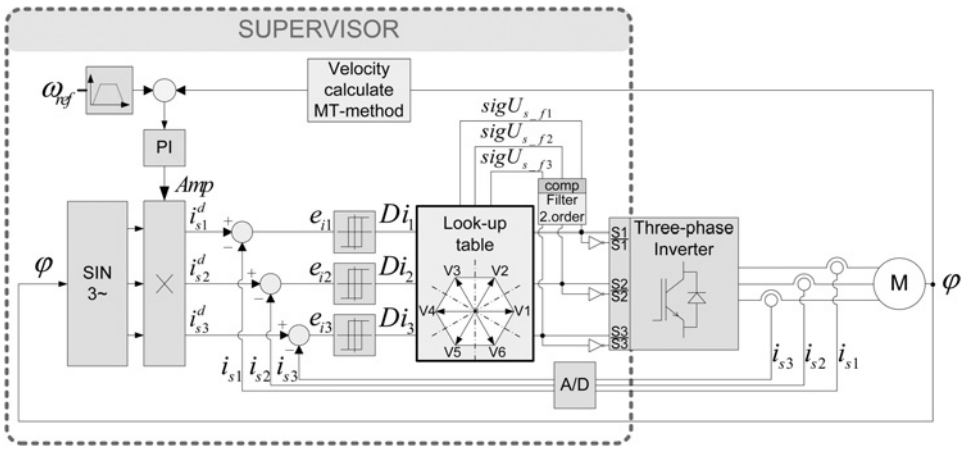

Fig. 1 *General control scheme of the BLAC motor*

doi: 10.1049/iet-pel.2010.0275

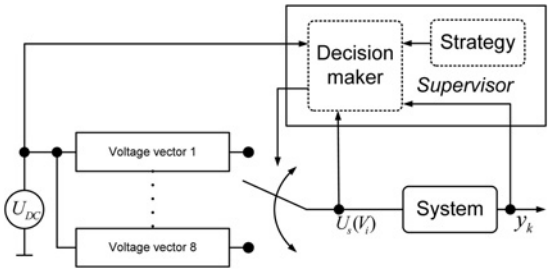

Fig. 2 *Hybrid control architecture*

Table 1 Stator voltage $u_s(V_i)$ definition

Voltage vector	Hexagon	S_1	S_2	S_3	u_{s1}	u_{s2}	u_{s3}
V_0		0	0	0	0	0	0
V_1		1	0	0	$2/3U_{DC}$	$-1/3U_{DC}$	$-1/3U_{DC}$
V_2		1	1	0	$1/3U_{DC}$	$1/3U_{DC}$	$-2/3U_{DC}$
V_3		0	1	0	$-1/3U_{DC}$	$2/3U_{DC}$	$-1/3U_{DC}$
V_4		0	1	1	$-2/3U_{DC}$	$1/3U_{DC}$	$1/3U_{DC}$
V_5		0	0	1	$-1/3U_{DC}$	$-1/3U_{DC}$	$2/3U_{DC}$
V_6		1	0	1	$1/3U_{DC}$	$-2/3U_{DC}$	$1/3U_{DC}$
V_7		1	1	1	0	0	0

literature on how the family of feedback functions should be selected [9].

4 System analysis and control

4.1 System analysis

The basic circuit of the voltage source inverter (VSI) feeding a Y-connected three-phase load, where the load has been modelled by a phase resistance, inductance and induced voltages. The voltage equation of the Y-connected three-phase load is

$$u_{sk}(V_i) = R_s\, i_{sk} + L_s \frac{\mathrm{d}i_{sk}}{\mathrm{d}t} + e_{sk}; \quad k = 1, 2, 3, \quad i = 0, 1, \ldots, 7 \tag{4}$$

where V_i represent the voltage vectors (Fig. 3) and the phase currents satisfy the linear condition

$$i_{s1} + i_{s2} + i_{s3} = 0 \tag{5}$$

The considered control problem is the tracking of a three-phase current reference signal. After the current control error is defined $\Delta \boldsymbol{i}_s = \boldsymbol{i}_s^d - \boldsymbol{i}_s$, (4) rewritten in error form becomes

$$L_s \frac{\mathrm{d}}{\mathrm{d}t}\Delta \boldsymbol{i}_s + R_s, \quad \Delta \boldsymbol{i}_s = \boldsymbol{u}_s(\boldsymbol{V}_i) - \boldsymbol{e}_s, \quad i = 0, 1, \ldots, 7 \tag{6}$$

which contains all the disturbances (exogenous and endogenous) action on the system.

The basic principle of the current control is to manipulate the input voltage vectors $\boldsymbol{u}_s(\boldsymbol{V}_i)$ so that the desired current is produced by the inverter. This is achieved by choosing an inverter switch combination S_i that drives the stator current vector by directly applying the appropriate inverter voltages $\boldsymbol{u}_s(\boldsymbol{V}_i)$ to the BLAC machine windings (4). The switch positions of the three-phase inverter are described using the logical variables V_i, depending if the switch S_i is ON or OFF. Each variable corresponds to one phase of the inverter. Three-phase inverter can produce eight voltage vector combinations; two of them are zero vectors and the remaining six are active vectors (Fig. 3).

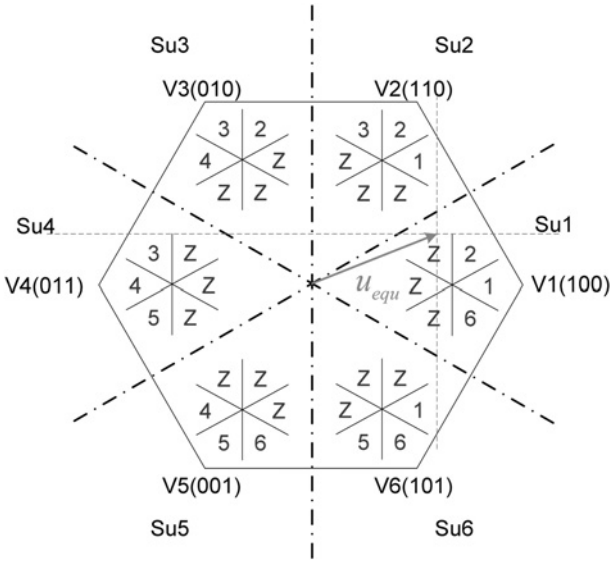

Fig. 3 *Stator voltage $\boldsymbol{u}_{equ}$ sector allocation spaces*

The energy flow between the input and output side of the three-phase inverter is controlled by the switching matrix. By introducing the binary variables S_i which are '1', if particular switch S_i is ON, and '0' if switch S_i is OFF ($i = 1, 2, 3, \ldots, 6$) the behaviour of the switching matrix can be described by the three-dimensional vector $\boldsymbol{u}_s = U_{DC}\boldsymbol{L}\boldsymbol{S}_i$, where matrix $\boldsymbol{L}$ and vector $\boldsymbol{S}$ (S_1, S_2, S_3) are defined as [10]

$$\boldsymbol{L} = \begin{bmatrix} 1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \end{bmatrix} \tag{7}$$

$$\boldsymbol{S}^{\mathrm{T}} = \begin{bmatrix} S_1 & S_2 & S_3 & \bar{S}_1 & \bar{S}_2 & \bar{S}_3 \end{bmatrix}$$

S_1, S_2, S_3 are the upper switches states of the inverter ($S = 1$ means switch is closed, $S = 0 = \bar{S}$ means switch is open). It essentially shows that this particular switching matrix is able to generate three independent control actions denoted as the components S_1, S_2 and S_3 of the control vector $\boldsymbol{u}_s(\boldsymbol{V}_i) = U_{DC}[S_1, S_2, S_3]^{\mathrm{T}}$. The components, that is, switch position of the inverter are generated by the look-up table of FPGA controller.

4.2 Discrete event control

To consider a hysteresis controller as a discrete-event dynamic system, it allows focusing on the switching actions and enables a better understanding of the controller design. A discrete-event system reacts only if an event is recognised. To control the current $\boldsymbol{i}_s$, the sector of the drive voltage $\boldsymbol{u}_{\mathrm{equ}}$ is recognised first, and based on the known sector, the input voltage vector $\boldsymbol{u}_s(\boldsymbol{V}_i)$ (the transistor

switching pattern) is selected for the current control, which takes into account the current control error related to the Lyapunov stability condition

$$V = (1/2)\Delta \boldsymbol{i}_s^{\mathrm{T}} \Delta \boldsymbol{i}_s = (1/2)(\boldsymbol{i}_s - \boldsymbol{i}_s^d)^{\mathrm{T}}(\boldsymbol{i}_s - \boldsymbol{i}_s^d) \quad (8)$$

The stability requirement is fulfilled if the control low can be selected as such that the derivative of the Lyapunov function candidate is negative $\dot{V} = \Delta \boldsymbol{i}_s^{\mathrm{T}} \Delta \dot{\boldsymbol{i}}_s \leq 0$. Derivatives of the current control error (6) may be expressed with the voltage equation

$$(\mathrm{d}/\mathrm{d}t)(\boldsymbol{i}_s - \boldsymbol{i}_s^d) = (1/L_s)(-\boldsymbol{e}_s - R_s \boldsymbol{i}_s + \boldsymbol{u}_s(\boldsymbol{V}_i)) - (\mathrm{d}/\mathrm{d}t)\boldsymbol{i}_s^d \quad (9)$$

where $\boldsymbol{i}_s^d$, $\boldsymbol{i}_s$ are desired and actual motor current, $\boldsymbol{u}_s(\boldsymbol{V}_i)$ is voltage control input, $R_s \boldsymbol{i}_s$ is resistive voltage drop and $\boldsymbol{e}_s$ is exogenous disturbance. For $\mathrm{d}(\Delta \boldsymbol{i}_s)/\mathrm{d}t = 0$ the equivalent control voltage can be expressed as [11]

$$\boldsymbol{u}_{\mathrm{equ}} = \boldsymbol{e}_s + R_s \boldsymbol{i}_s + L_s(\mathrm{d}/\mathrm{d}t)\boldsymbol{i}_s^d \quad (10)$$

and derivative of the Lyapunov function is presented with the equivalent control and control input voltage $\boldsymbol{u}_s(\boldsymbol{V}_i)$ as

$$\dot{V} = (\boldsymbol{i}_s - \boldsymbol{i}_s^d)(\boldsymbol{u}_s(\boldsymbol{V}_i) - \boldsymbol{u}_{\mathrm{equ}})/L_s < 0 \quad (11)$$

To consider space-vector representation of the stator voltage $\boldsymbol{u}_s(\boldsymbol{V}_i)$, the voltage is represented as vector that rotates around the origin. Six active switching vectors of the three-phase transistor inverter represent the six active output voltage vectors denoted as $V_1, \ldots, V_6$. V_0 and V_7 are two zero voltage vectors. According to signs of the phase voltages u_{s1}, u_{s2} and u_{s3}, the phase plane is divided into six sectors denoted by $S_{u1}, \ldots, S_{u6}$ (Fig. 3).

In regards to the situation (Fig. 3), the stator voltage space vector $\boldsymbol{u}_{\mathrm{equ}}$ is in the sector S_{u1}. In this sector, logical voltage vectors $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_6$ and $\boldsymbol{V}_7$ are selected for the current control. $\boldsymbol{V}_0$, $\boldsymbol{V}_7$ are two zero vectors, while $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_6$ are the three nearest adjacent live output voltage vectors for this sector. With the use of the discrete event system theory, five output voltage vectors $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, $\boldsymbol{V}_6$ and $\boldsymbol{V}_7$ are recognised as discrete states of the system. Events represent allowed transitions among the discrete states. Allowed switchings are determined via stability issue.

A novel, discrete event current controller evaluates the transistor switching pattern $\boldsymbol{S}(S_1, S_2, S_3)$ of inverter from the sign of the current error, sign $(\boldsymbol{i}_s - \boldsymbol{i}_s^d)$ and the sign of actual voltage sector sign($\boldsymbol{u}_{\mathrm{equ}}$).

When U_{dc} has magnitude high enough such that $\dot{V} \leq 0$, then $V \to 0$ and $\boldsymbol{i}_s \to \boldsymbol{i}_s^d$. S_1, S_2 and S_3 represent the switching state of the three-phase power converter. Notice that if S_1, S_2, S_3 equal to zero simultaneously, no current is delivered to the BLAC motor. Moreover, the manifold $\Delta \boldsymbol{i}_s = 0$ is reached in a finite time, and if the switching is fast enough, the trajectories stay in that manifold all the time [11].

5 Switching strategy

Bang–bang hysteresis current control is the fastest and robust method due to a very simple implementation. A simple hysteresis controller is needed only to compare two input data. Bang–bang hysteresis current control's advantage is non-controlled switching frequency of switching elements. In some cases, this can cause very fast switching–chattering, which is the main obstacle for practical application of sliding mode control. In proposed study switching frequency can be reduced only if the hysteresis limits increase, however, the chattering of the current and torque increase as well. Bang–bang method uses hysteresis to set the maximal switching frequency. Discrete event system (DES) control includes hysteresis and look-up table to reduce a switching frequency that is crucial in converter losses. Comparison of the DES, bang–bang and sliding mode does not consider the decision of the supervisor. Supervisor provides stable and secure operation of the system.

The proposed logical event-driven BLAC current control can be realised in the form described in Table 2, where states of current control error are presented by sign (D_i) and currently active voltage sector is presented by sign (U_{s_f}). Three bits value of sign (U_{s_f}) consists of signs of three filtered stator phase voltage.

To further improve the presentation, active voltage vectors are marked in Table 2 with grey background. Because the transition between inverter switch states is performed by switching only one inverter leg, switching frequency and current chattering (and consequently torque chattering of BLAC motor) are reduced.

In the proposed new developed switching voltage space vector modulator voltage vectors V_i can be mapped into the three-phase plane as shown above in Fig. 3. This provides a geometric interpretation of the voltages that can be produced by the inverter. The driving signal of inverter switches can be generated with FPGA circuit. The considered control task is a tracking of three-phase current reference signal. The current error is computed in a vector form and the switching configuration is related to keep the error inside a two dimensional sign(u_i) and sign(Vi_s) tolerance region. The zero voltage control vector can be consciously used to reduce the transistor's switching frequency [7].

6 Implementation and protection issue

An important advantage of using FPGA for the controller is that some additional functions like protections, steering, monitoring and so on can be added without any additional resources and almost any drawback in performance, shown in Fig. 1. The proposed hybrid BLAC motor control on FPGA, allows implementation of the decision logic and control operations simultaneously.

In this way, there is almost no drawback in the controller performance because the control logic is executed as if there are no protections. Even more, the protections are executed continuously, instead of the periodic execution in a DSP. DSP solutions must keep the protections resources

Table 2 Look-up table

Sign U_{s_f} Sign D_i		S_{u1} 100	S_{u2} 110	S_{u3} 010	S_{u4} 011	S_{u5} 001	S_{u6} 101
Sdi0	000	V7	V0	V0	V7	V0	V7
Sdi1	100	V1	V1	V0	V7	V0	V1
Sdi2	110	V2	V2	V2	V7	V0	V7
Sdi3	010	V7	V3	V3	V3	V0	V7
Sdi4	011	V7	V0	V4	V4	V4	V7
Sdi5	001	V7	V0	V0	V5	V5	V5
Sdi6	101	V6	V0	V0	V7	V6	V6
Sdi7	111	V7	V0	V0	V7	V0	V7

doi: 10.1049/iet-pel.2010.0275

at a minimum because the main control is stopped while a protection is verified. In fact, any algorithm can be added to the control as long as there are available resources.

To substitute the common DSP solutions with FPGA-based ones, it means a trade-off between the DSP capacity for arithmetic operations and FPGA concurrency. To explicit FPGA concurrency, new control algorithms must be developed, because to adapt the DSP-oriented to FPGA would not mean any special advantage. These new algorithms can be quite simple, like DES control proposed, although they must be designed from the concurrency point of view.

6.1 Hardware of hybrid controller

The proposed approach is based on fast parallel processing and it is suitable for a FPGA implementation. In such implementation, it would be possible to reproduce near ideal switching mode process. However, with FPGA implementation, designer has a difficult task to characterise and describe the hardware architecture that corresponds to the chosen control algorithm [12]. FPGA designers must follow an efficient design methodology in order to benefit from the advantages of FPGAs and their powerful CAD tools. From a software point of view, hardware description language (HDL) modelling system is based on the use of variables that request logic values, too.

A low-cost Xilinx Spartan 3 FPGA that contains 1.2 M logical gates and includes a 50 MHz oscillator has been used as a target component for the implementation of the controller. The architecture of each control algorithm is designed according to an efficient methodology that offers considerable design advantages, such as reusability, reduction of development time and optimisation of the consumed resources. Each control algorithm is partitioned into elementary modules, which are easier to develop and are more functional.

Fig. 4 presents the general structure of the different elementary modules. As shown in Fig. 4, Xilinx Spartan XC3S1200E is used to implement the BLAC motor controller. This motor control intellectual property (IP) is divided into three parts. The first part is the driver's part with ADC and DAC management modules, incremental module for speed and position measurement and RS 232 module for connection of host PC equipment with Matlab/Simulink program environment. The second part includes the PI-speed motor controller. Output of speed controller is a measure for the desired torque of BLAC motor that multiplies the three-phase reference currents of machine. The currents phases depend on rotor position. The third part includes the look-up table with hysteresis current controller and an average output voltage of BLAC motor synchronisation – voltage sector selection (Fig. 4).

6.2 Management and protection

Current amplitude, motor speed, DC-link and motor temperature are monitored by the supervisor. The supervisor can affect the parameters and the reference values when any of the measured values is critical. If the system overloads, the supervisor immediately initiates the procedure to protect the system. Protection algorithm starts with modifying the parameters and reference values. When modifying of the parameters and reference values cannot solve the problem, the supervisor affects the state of the inverter directly.

The steering function determines the converter's operation mode. The three main possible modes are of concern: Ready, Operate or Error. They are considered as discrete states of the monitoring function. Initially, the Begin mode is active. Turn the main switch (ON/OFF) to ON, enable search for absolute position of the rotor that is term for the transition to state Ready. Inverter voltage is ensured in this state. From the state Ready, it is possible to start the system (Operate) by pressing the START button. Operate mode allows the change of all free parameters and reference values. Stopping the system is possible by pressing the STOP button. Stopping mode resets all of the parameters (puts them on reference values) and puts the current and speed reference to zero. If rotor is stopped, the system reverts to the Ready mode. In these three states Ready, Operate and Stopping, the system constantly monitors values of current, inverter voltage and temperature and rotor speed. If any of these values are outside the permitted quantities, the system continues in Warning mode. Warning mode is intended to alert the user that the system is in a limit range of the safe system activity. In the state Error, it is the first, to initiate the RESET, which causes the state Stopping. If stopping system is successful then the system returns to the state Ready, otherwise turn off the main switch. For system reboot, servicer should eliminate the error which causes a critical state of the system.

6.3 Implementation in ISE (VHDL code)

Such a scheme for operation occupies 35% of the 'number of 4 input LUTs' FPGA circuit and 67% of 18-bits multipliers.

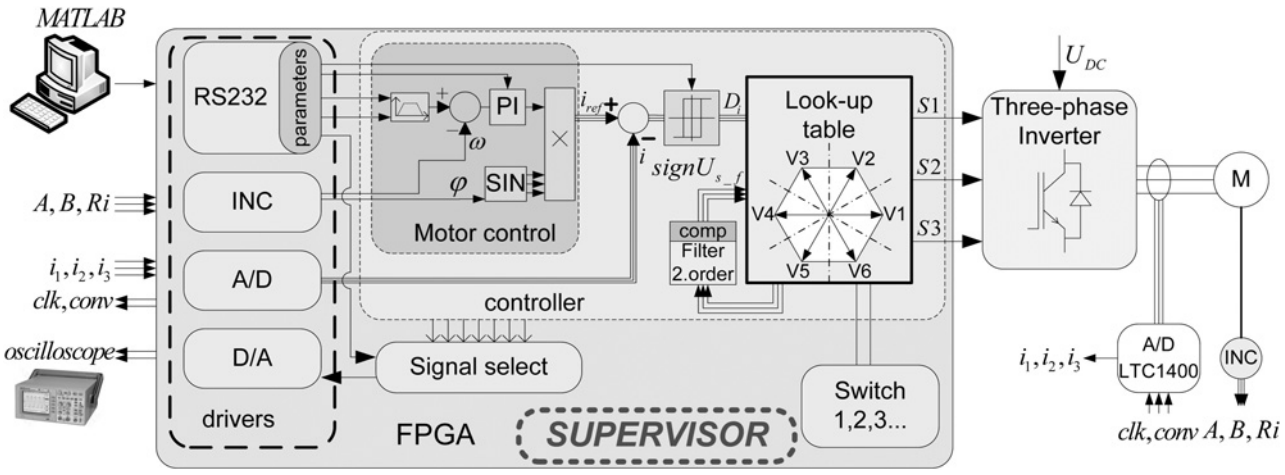

Fig. 4 *FPGA controller of the BLAC motor*

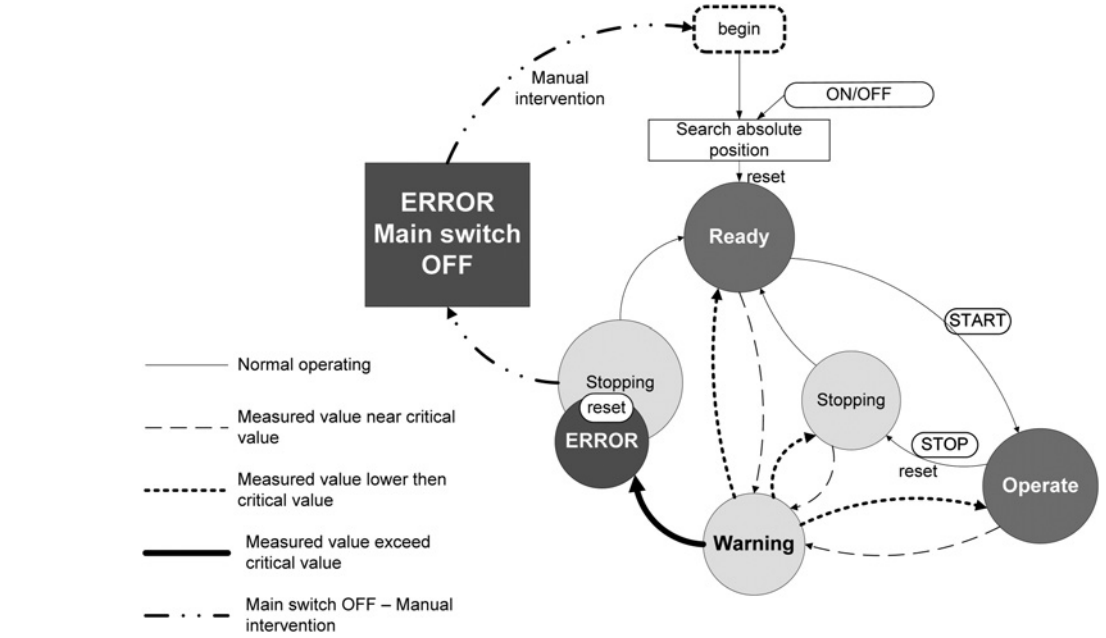

Fig. 5 *State computer – SUPERVISOR*

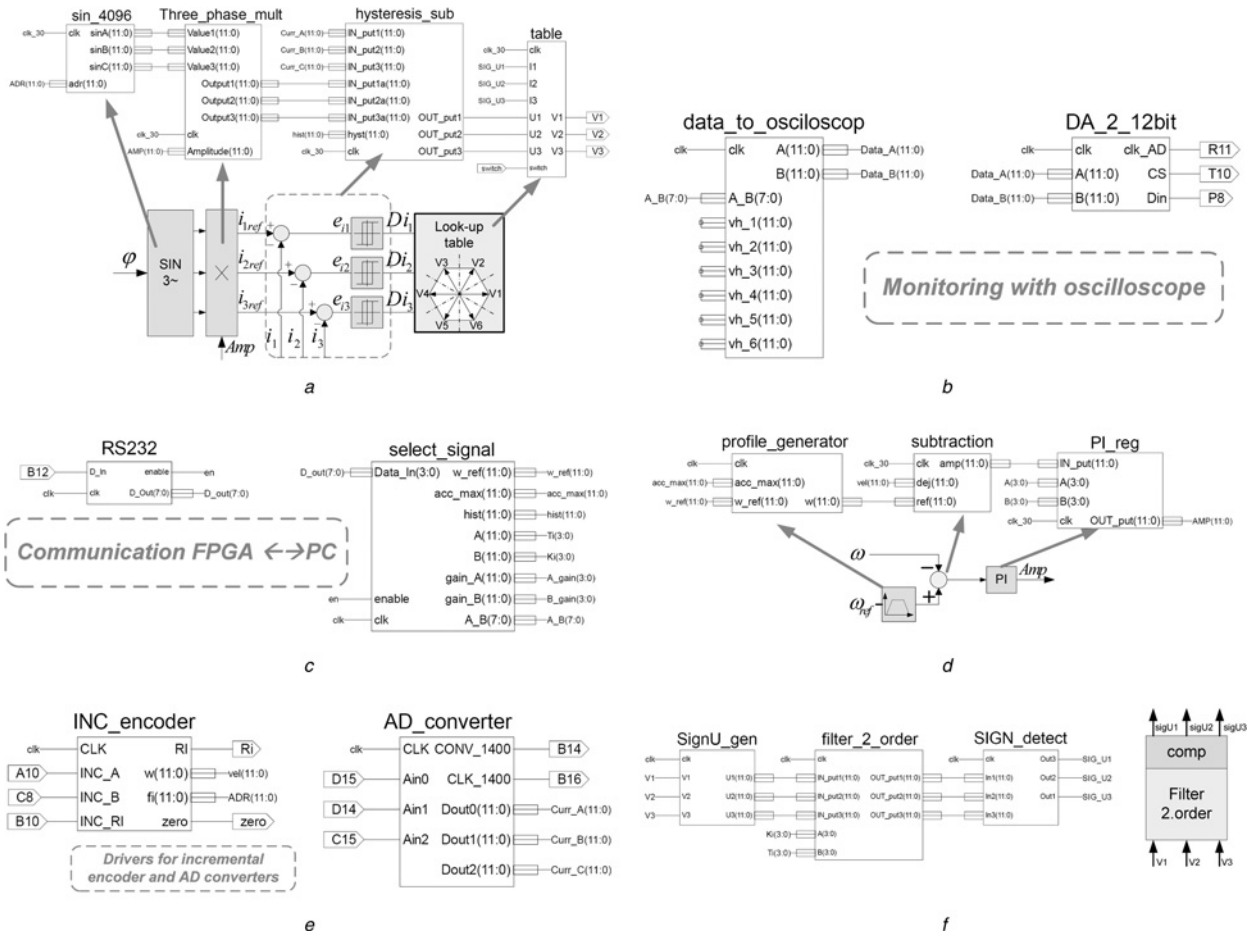

Fig. 6 *Implementation in ISE*

a Current control with look-up table
b Data from FPGA to oscilloscope
c RS232 communication
d Amplitude generating
e Incremental encoder and A/D converter drivers
f Sign *U* calculation

doi: 10.1049/iet-pel.2010.0275

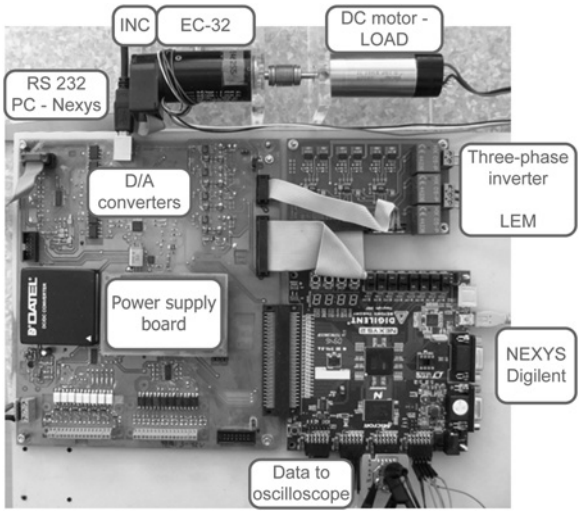

Fig. 7 *Experimental system*

Very high speed integrated circuit hardware description language (VHDL) code has been created in Xilinx ISE software (Fig. 5). Software scheme is divided into individual blocks for better review (Fig. 6). It is composed of a data path and a control unit coded in VHDL. The data path is composed of gain operators such as adders, multipliers, multiplexers and registers. The data transfer between these operators is managed by a control unit, which is synchronised with the clock signal (CLK). The control unit of the developed modules is always activated via Start pulse signal. When the computation time process is over, an End pulse signal indicates that the data outputs of the module are ready.

This generic structure can be easily introduced in an upper hierarchical level architecture and it can also be used for future design. Basic step time (clock) for execution of arithmetic operations is 30 ns. Current measurement is limited, with a conversion time of A/D converters, to 2.5 μs. Entire scheme (data lines) is based upon 12-bits signed numbers. The protection of three-phase inverter (dead time) is provided by the transistors drivers. Fig. 7 shows the composition of the experimental model.

7 Experimental results

To test the proposed FPGA-based controller, the experiments have been carried out on in-house built FPGA prototyping platform. In all simulations and experimental results, the BLAC motor from Maxon, type EC32 with parameters as given in Table 3 was used. FPGA controller has the diagnostic features that are necessary for drive installation, test problem detection and elimination. The control algorithm is executed every 2.5 μs, and the switching

Table 3 BLAC motor parameters

$U_n = 18$ V	nominal voltage
$I_n = 490$ mA	no load current
$I_{max(5000rpm)} = 4.9$ A	maximum continuous current at 5000 rpm
$R_s = 0.56\ \Omega$	terminal resistance phase to phase
$L_s = 0.09$ mH	terminal inductance phase to phase
$J = 20$ gcm^2	rotor inertia
$\Psi_{PM} = 0.205$ Vs	rotor flux
$\tau_M = 6.6$ ms	mechanical time constant

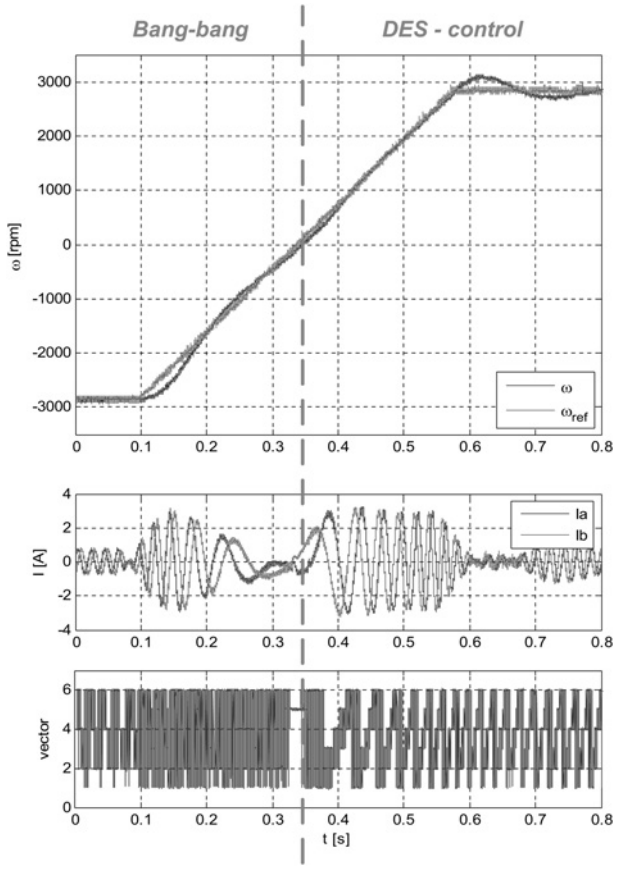

Fig. 8 *Active voltage vectors at progressive change of reference speed*

frequency of three-phase inverter is set with the tolerance band of the hysteresis current control. The control of both, the speed and applied torque, is possible; thus the hardware in the loop operation can also be performed.

The experimental results are illustrated in Figs. 8–10. The results are recorded with an oscilloscope and consequently the measured results are contaminated with noise.

Fig. 8 shows the transient of speed (ω) currents (i_a, i_b) and voltage vectors (spectrum) $V_i(S_1, S_2, S_3)$ of three-phase inverter. Starting with classical bang–bang regulated and at change speed sign is switched to the proposed hybrid DES. Pulse pattern of voltage vector $V_i(S_i)$ changes transients

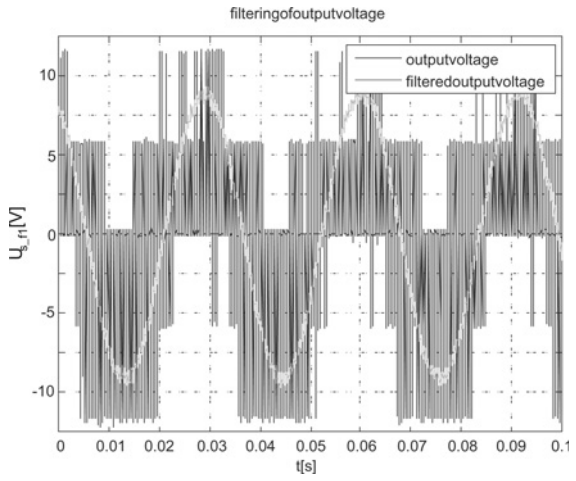

Fig. 9 *Filtering of output voltage for one phase*

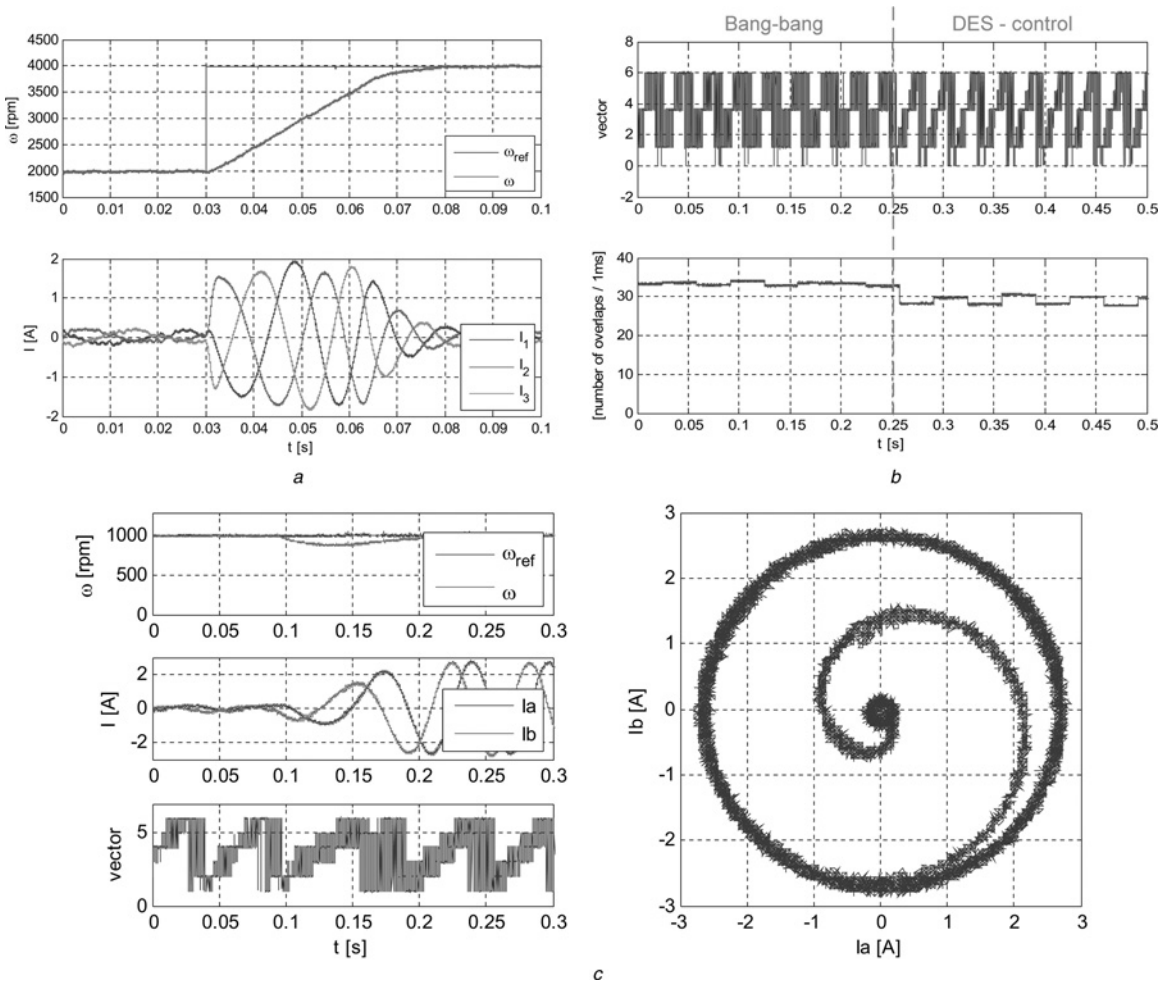

Fig. 10 *Experimental results*

a Step response
b Switches number of switching elements at 2000 rpm
c Torque perturbation response

from the conventional bang–bang current control to the hybrid DES current control of inverter. Parameters of PI-regulator define speed response of motor. In this case, the slower speed response makes more explicit currents changes.

Fig. 9 shows the transients of output voltage $\boldsymbol{u}_s(\boldsymbol{V}_i)$ and average filtered output voltage for one phase of the inverter. This signal is used for voltage vector selection in look-up table. Based on this simplified close-loop, the transfer function is expressed as

$$\frac{U_{s\_f}(s)}{U_s(s)} = \frac{sB + A}{s^2 + sB + A}; \quad B = 1400, \quad A = 490\,000 \quad (12)$$

This transfer function corresponds to a second-order system. The observation dynamic is then set using A and B coefficients. Step response of reference speed is shown in Fig. 10*a*. Speed controller defines speed response and currents amplitude.

DES control successfully reduces the number of switching transistors. Fig. 10*b* shows the number of switches within the interval 1 ms. Fig. 10*b* shows the number of switching at a constant motor's speed of 2000 rpm. The difference between the hysteresis and DES control is the highest at low velocities. With increasing speed this difference decreases. However, reducing of switching frequency, increases current waving. Fig. 10*c* shows current, speed and vector response in the case of load perturbation. Only active voltage vectors are shown, which are often used to present the effect of torque perturbation.

8 Conclusions

The idea of the hybrid-based control of event-driven systems is used for the design of event-driven current (torque) controller, auxiliary steering and protection functions for a BLAC servo drives. Individual control functions have been designed with the use of the proposed approach and integrated into the overall functionality description of the inverter.

In this study, the hybrid control problem of BLAC motor has been addressed. The non-linear behaviour of the system limits the performance of chosen bang–bang controllers that are used for this purpose. This paper has successfully demonstrated the design, stability analysis, simulation and tests of the Lyapunov technique approach for the DES control of the BLAC drive. The feedback system is globally asymptotically stable, in relationship to the Lyapunov method. The transient state and the steady-state performances of the logical-based controller have been improved via the Lyapunov stability. Consequently, high

doi: 10.1049/iet-pel.2010.0275

performance dynamic is obtained, despite the presence of parameter uncertainties or disturbances.

The simulation and experiments confirm the potential of the presented approach: traditional coding efforts are significantly reduced on the one hand, and on the other hand the control algorithm can be verified offline. Formal mathematical background of the proposed approach and its correspondence to the conventional control system theory opens further possibilities for the design, simulation and formal analysis of the DESs. The proposed approach offers a promising technique for design of complex and timely critical algorithms. On the one hand, the future research is oriented towards the optimisation of the introduced motion control strategies, and on the other hand towards the formalisation of analysis and control design methods.

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