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PSML: parallel system modeling and simulation language for electronic system level

November 2018 · The Journal of Supercomputing

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 Sima Sinaei ·  Omid Fatemi

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Article

Feb 2018 · IEICE Transactions on Information and Systems

 Shimpei Sato ·  Ryohei Kobayashi ·  Kenji Kise

LSIs are generally designed through four stages including architectural design, logic design, circuit design, and physical design. In architectural design and logic design, designers describe their target hardware in RTL. However, they generally use different languages for each phase. Typically a general...

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 Janche Sang ·  Che-Rung Lee ·  Vernon Rego ·  Chung-Ta King

Modern graphics processing units (GPUs) offer much more computational power than recent CPUs by providing a vast number of simple, data-parallel, multithreaded cores. In this study, we focus on the use of a GPU to perform parallel discrete-event simulation. Our approach is to use a modified service time...





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Chapter

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 R. Dömer ·  G. Liu ·  T. Schmidt

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Conference Paper

Jun 2017

 Tim Schmidt ·  Guantao Liu ·  Rainer Dömer

Most parallel SystemC approaches have two limitations: (a) the user must manually separate all parallel threads to avoid data corruption due to race conditions, and (b) available hardware vector units are not utilized. In this paper, we present an advanced compiler infrastructure for automatic parallelization of...

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Article

May 2017 · ACM Transactions on Modeling and Computer Simulation

 Elsa Gonsiorowski ·  Justin M. Lapre ·  Christopher D. Carothers




Gate-level circuit simulation is an important step in the design and validation of complex circuits. This step of the process relies on existing libraries for gate specifications. We start with a generic gate model for Rensselaer's Optimistic Simulation System, a parallel discrete-event simulation framework. This...

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Feb 2017 · Computing

 Alireza Poshtkahi ·  M. B. Ghaznavi-Ghouschi ·  Kamyar Saghafi

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