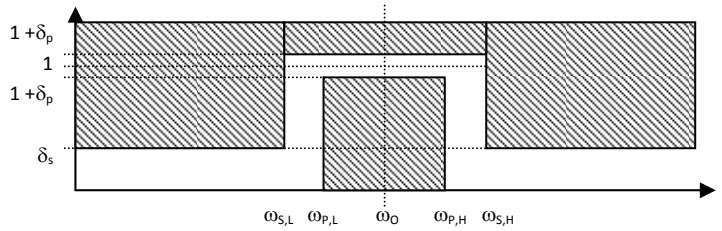
We wish to implement a band-pass filter to demodulate an AM radio station with frequency content in the range 726−734kHz (content in this range should be accepted ±1%). We need to reject frequencies below 720kHz and above 740kHz by at least 40dB. We use a DSP system with a sampling frequency of 2MHz.

Our DSP takes 1 clk cycle for addition and 5 clk cycles for multiplication (assume other operations are zero cost). This DSP is available in versions with clk speeds of: 1MHz, 2Mhz, 5Mhz, 10MHz, 20Mhz, 50Mhz, 100MHz, 200Mhz, 500Mhz, 1Ghz, 2GHz. Faster DSPs are more expensive and use up batteries faster.

A. Sketch the filter specifications. What are $\omega_{p,L}$, $\omega_{p,H}$ and $\omega_{s,L}$, $\omega_{s,H}$.

Answer:



$f_{S,L}$ = 720kHz → $f_{S,Lnorm}$= 720kHz/2MHz = .360 cyc/sample → $\omega_{S,Lnorm}$= .360 (2π) rad/sample
$f_{P,L}$ = 726kHz → $f_{P,Lnorm}$= 726kHz/2MHz = .363 cyc/sample → $\omega_{P,Lnorm}$= .363 (2π) rad/sample
$f_{P,H}$ = 734kHz → $f_{P,Hnorm}$= 734kHz/2MHz = .367 cyc/sample → $\omega_{P,Hnorm}$= .367 (2π) rad/sample
$f_{S,H}$ = 740kHz → $f_{S,Hnorm}$= 740kHz/2MHz = .370 cyc/sample → $\omega_{S,Hnorm}$= .370 (2π) rad/sample
δ_S → given by 40dB spec $\delta_S = 10^{-40/20} = .01$
δ_P → 1% so δ_P → 0.01

B. Calculate ω_c, ω_0 for the BPF. Calculate the ideal BPF.

Answer

$\omega_{\text{lower cutoff}} = (\omega_{S,Lnorm} + \omega_{P,Lnorm})/2 = .3615(2\pi)$ rad/sample
$\omega_{\text{upper cutoff}} = (\omega_{P,Hnorm} + \omega_{S,Hnorm})/2 = .3685(2\pi)$ rad/sample
$\omega_O = (\omega_{c,L} + \omega_{c,H})/2 = .365(2\pi)$ rad/sample
$\omega_{c,L} = \omega_O - \omega_{\text{lower cutoff}} = .0035(2\pi)$
$\omega_{c,H} = \omega_{\text{upper cutoff}} - \omega_O = .0035(2\pi)$
$TBW_L = (\omega_{P,Lnorm} - \omega_{S,Lnorm}) = .003(2\pi)$ rad/sample → .003 cyc/sample
$TBW_H = (\omega_{S,Hnorm} - \omega_{P,Hnorm}) = .003(2\pi)$ rad/sample → .003 cyc/sample

$h_{BP,IDEAL}[n] = 2\cos[n\omega_o][\omega_c/\pi]\text{sinc}[n\,\omega_c/\pi]$ per slide 20.17
$= 2\cos[n(0.730\pi)][.007]\text{sinc}[n(.007)]$

Note – filter is symmetric (Transition bands have same specification)

C. Choose a windowing function and window length for this filter.

Answer

40dB stop band specification → Hann is acceptable window (per slide 22.14)

For Hann: $1.56/L = TBW = .003$

$L = 1.56/.001 = 520 \rightarrow M = 2L+1 = 1041$

D. Calculate the expression for the FIR filter to implement this specification.

Answer

$h_{BP}[n] = h_{window}[n]\, h_{BP,IDEAL}[n]$

$= (0.5 + 0.5\cos(\pi(n-L)/L))(2\cos[(n-L)\omega_o][\omega_c/\pi]\text{sinc}[(n-L)\omega_c/\pi])$

$= (0.5 + 0.5\cos(\pi(n-520)/520))(2\cos[(n-520)(0.730\pi)][.007]\text{sinc}[(n-520)(.007)])$

E. To implement this filter as an FIR convolution, how many multiplies and additions are required per output sample.

Answer:

M = 1041

So convolution requires

M multiplies per sample	1041*5 clk/mult =	5205
M-1 additions per sample	1040*1 clk/add =	1040
Total		6245 clks/sample

F. What is the slowest clock speed DSP that can be used for this application using FIR convolution?

Answer:

2MHz sampling – Need processor > 6245*2MHz = 12.49GHz
None of the available processors will meet the need.

G. To implement this filter using FFT block processing, calculate how many multiplies and additions are required per output sample:
   i. for N= 2048
   ii. for N= 4096

Answer:

N=2048
M=1041
B=N-M+1 = 2048-1041+1 = 1008 - processing 1008 sample length blocks

FFT Mults	$(N/2)(\log_2 N-2)+1$	$(2048/2)(\log_2 2048-2)+1$	9217	*5	46085
FFT Adds	$N\log_2 N$	$2048\log_2 2048$	22528	*1	22528
Filter Mults	N	2048	2048	*5	10240
IFFT Mults	$(N/2)(\log_2 N-2)+1$	$(2048/2)(\log_2 2048-2)+1$	9217	*5	46085
IFFT Adds	$N\log_2 N$	$2048\log_2 2048$	22528	*1	22528
Overlap Adds	N	2048	2048	*1	2048

Total clocks per Blocks 149.5K
Clocks / samples =149.5K/B = 149.5K/1008 = 148.3 clocks/sample

N=4096
M=1041
B=N-M+1 = 4096-1041+1 = 3056 - processing 3056 sample length blocks

FFT Mults	$(N/2)(\log_2 N-2)+1$	$(4096/2)(\log_2 4096-2)+1$	20481	*5	102405
FFT Adds	$N\log_2 N$	$4096\log_2 4096$	49152	*1	49152
Filter Mults	N	4096	4096	*5	20480
IFFT Mults	$(N/2)(\log_2 N-2)+1$	$(4096/2)(\log_2 4096-2)+1$	20481	*5	102405
IFFT Adds	$N\log_2 N$	$4096\log_2 4096$	49152	*1	49152
Overlap Adds	N	4096	4096	*1	4096

Total clocks per Blocks 327.7K
Clocks / samples =327.7K/B = 327.7K/3056 = 107.2 clocks/sample

H. What is the slowest clock speed DSP that can be used for this application using DSP block processing?

Answer:

At N = 2048 min processor = 148.3*2MHz = ~0.3GHz so use 500Mhz (1GHz more likely)
At N = 4096 min processor = 107.2*2MHz = ~0.2GHz so use 500Mhz (likely do not need 1G)

I. What is the processing delay for the FIR?

Answer:

N=2048 ; CPU_f = 500MHz
Fs = 2MHz → Ts = 0.5×10^{-6} secs
$CPU_t = 2 \times 10^{-9}$ secs
Processing delay

Block delay = B* Ts = 1008 * 0.5×10^{-6} = .504msec
Filter delay = CLKS * CPU_t = 149.5×10^{3} * 2×10^{-9} =.299 msec

Delay = .803 msec

N=4096; CPU_f = 500MHz
Fs = 2MHz → Ts = 0.5×10^{-6} secs
$CPU_t = 2 \times 10^{-9}$ secs
Processing delay

Block delay = B* Ts = 3056 * 0.5×10^{-6} = 1.528msec
Filter delay = CLKS * CPU_t = 327.7×10^{3} * 2×10^{-9} =.655 msec

Delay = 2.183 msec