Carleton University,
Systems and Computer Engineering
SYSC 4405: Final Exam, December 13, 2008
Exam Number: 1

Instructions:

- This exam has **2** pages and **15** questions. Answer all questions.
- You have **180 minutes** to complete this exam.
- This is a closed book exam; however, you are permitted to bring one (1) 8.5” × 11” sheet of notes into the exam. You are permitted to use a non-programmable calculator. You may not communicate with anyone during the exam except the instructor.
- Write your answers on an examination booklet. *You may take this examination paper with you*

Background: You get a job working in an ultra secret lab which designs spy equipment for a national agency. The device you need to design will allow a secret agent to pass along a message through an innocent sounding voice phone message (this is also called *Steganography*). Here’s how it works: the agent speaks normally into the phone and talks about the weather. At the same time, a small device transmitts digital content into the phone using very soft (low amplitude signals). The signals are at frequencies of 81 Hz and 107 Hz.

You’re required to design the device at the receiving end. A small DSP based device is placed onto physical contact with the phone. It detects the received signals using a piezoelectric sensor and processes the data to detect the secret signals. The DSP system does not have any output. It stores signals encrypted in memory. Once the agent get’s back to a safe place, he or she can access the data (we don’t look at this part of the design in this exam).

Note: that such a simple scheme wouldn’t be used. Instead secret information would be spread into the voice spectrum.

To save power and battery life, the design is based on a 1 MHz clock DSP chip. For calculations based on this chip you may assume: 1) multiplications require 5 clock cycles. 2) additions require 1 clock cycle.

1. (1 point) Your exam is exam number **1**. Write down this number.

2. (5 points) The detector system is built using a DSP system. **Sketch the DSP system components as a block diagram.** On your diagram, label the: a) Sample/Hold, b) Analog Low pass filter, and c) Clock.

3. (5 points) A 1 kHz sampling rate is used. **Choose a reasonable antialiasing filter:** is it HP, LP, BP? what is the cut-off frequency? **Briefly ($\leq$ 20 words) explain your choice.**

4. (5 points) In this circuit, we use an antialiasing filter designed with analog components. **Is it possible to build an antialiasing filter using DSP techniques? Why or why not**

5. (5 points) The A/D converter encodes values between -2 V and 2 V into a 16 bit range. The speach signal is uniformly distributed over the range of 1 V peak-to-peak. **What is the signal to noise ratio due to quantization?**

6. (5 points) One initial problem is interference with 60 Hz power line noise. We want to design a notch filter, $H_{NF}(z)$, to remove it. $H_{NF}(z)$ has zeros at the frequency corresponding to 60 Hz. Poles are placed right next to the zeros, at 99% of the radius of the zeros in the z-plane. **Calculate the location of the poles and zeros, and sketch the pole/zero plot of $H_{NF}(z)$.**

7. (5 points) $H_{NF}(z)$ is designed to have a gain of 1.0. **What is the magnitude of $H_{NF}(z)$ at a frequency of 60 Hz? 61 Hz?**

8. (5 points) **Sketch the block diagram to implement $H_{NF}(z)$.**

9. (5 points) Based on the 1 MHz DSP CPU described, **how many clock cycles are requried for each sample processed by $H_{NF}(z)$?**

10. (5 points) **Characterize the filter $H_{NF}(z)$ using the following properties:**

linear	memoryless
shift-invariant	stable
causal	LSI
minimum phase	linear phase

11. (5 points) In order to detect the secret tones, we require a band pass filter which passes frequencies of ± 5 Hz of the centre frequency, and stops frequencies of ± 20 Hz of the centre frequency. The stop band attenuation must be less than 0.1% and the pass band deviation must be less than 10%. **Sketch the filter requirements for the 81 Hz tone.**

12. (10 points) **Design a BPF which meets the filter requirements** in the previous question.

13. (5 points) We use overlap-add block processing to implement this filter, using an FFT size of 1024. **Sketch block processing process**; indicate the size of all blocks.

14. (5 points) Using block processing, **how many DSP clock cycles** are required per input sample to implement the band pass filter.

15. (5 points) Assume the speech signal amplitude (1 V peak-to-peak, uniformly distributed) is uniformly distributed over the frequency range from 0 Hz to 5 kHz. The secret tones are very soft (assume 10 mV peak-to-peak, uniformly distributed). Consider the speach to be noise, **calculate a signal to noise ratio, assuming the BPF is ideal with a bandwidth of ± 15 Hz from the centre frequency.**

16. (5 points) **Comment briefly (≤ 30 words) on the reliability of this detection scheme.**