Biopotential Amplifiers: imperfections

DC Amplifier imperfections

- Common mode gain
- Power supply rejection
- Offset Voltage
- Bias Current
- Differential Bias Current
- Finite Input Impedance
- Finite Input / Output Range

AC imperfections

- Unity gain frequency
- Slew Rate
- Noise

Common mode gain

An instrumentation amplifier is designed to measure differential voltage, but the (often large) common mode voltages can “leak” onto the output.

Amplifier Gain may be divided into a

- Differential Gain (A_d)
- Common Mode Gain (A_{cm})
- Output: $V_o = A_d (V_d) + A_{cm} (V_{cm})$
- where: $V_d = V_+ - V_-$ (differential voltage)
  $V_{cm} = ½(V_+ + V_-)$ (common mode voltage)

Common mode rejection ratio (CMRR)

- $CMRR = A_d/A_{cm}$
- Normally in dB ($20\log_{10} A_d/A_{cm}$) my be up to 100dB

How to measure

1) Set $V_+ = V_- \Rightarrow$ Measure A_{cm}
2) Set $V_+ = -V_- \Rightarrow$ Measure A_d

Amplifiers

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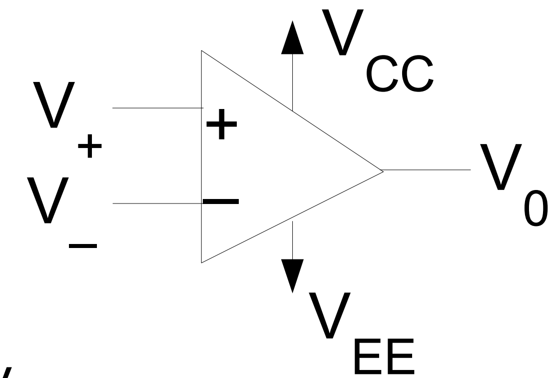
Power supply rejection

In a similar way to the common mode voltage, variability on the power supply can be seen on the output

$V_o = A_d (V_d) + A_{cm} (V_{cm}) + A_{ps} (\Delta V_{cc})$



where: ΔV_{cc} changes in the supply voltage

A_{ps} gain on power supply signals

Measurement

3) Set $V_+ = V_-$, vary V_{cc} ⇒ Measure $A_{ps} = \Delta V_o / \Delta V_{cc}$

Power supply rejection ratio

- PSRR = A_{ps}/A_d

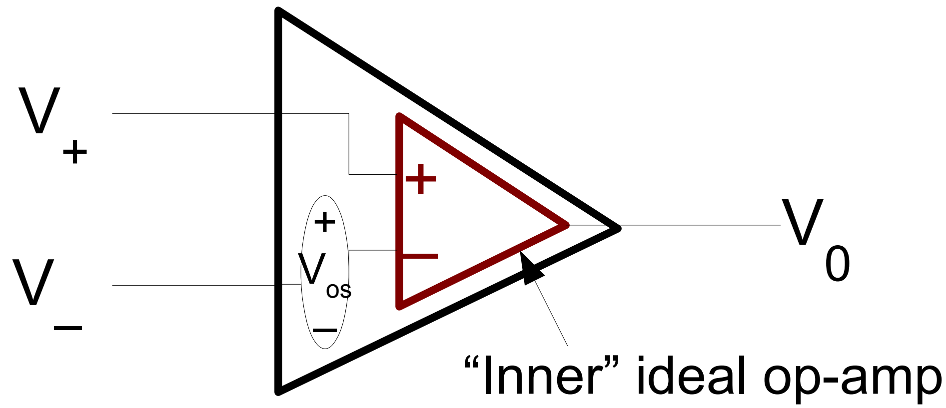
PSRR is an issue

- for AC supplied circuits (Variability in power from AC supplies)
- from digital switching which is coupled onto power supply

Offset Voltage

The offset voltage acts like a small battery (μV) in front of ideal op amp

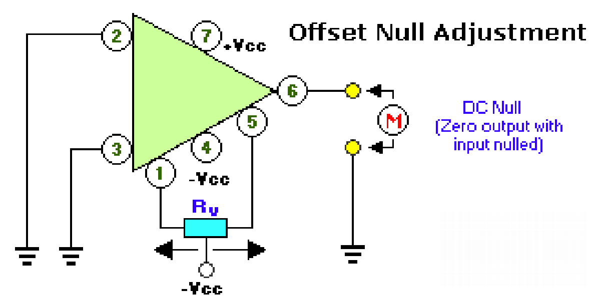
This effect means that if we set the inputs together ($V_+ = V_-$), we won't get zero



Offset voltage is smaller with BJT designs + higher with CMOS

Compensation

- Older Op amps (741) have nulling terminals
- Newer technique is laser trimming at wafer stage (eg OP07)
- Note: V_{os} drifts with time/temperature. This can't be nulled with trimming

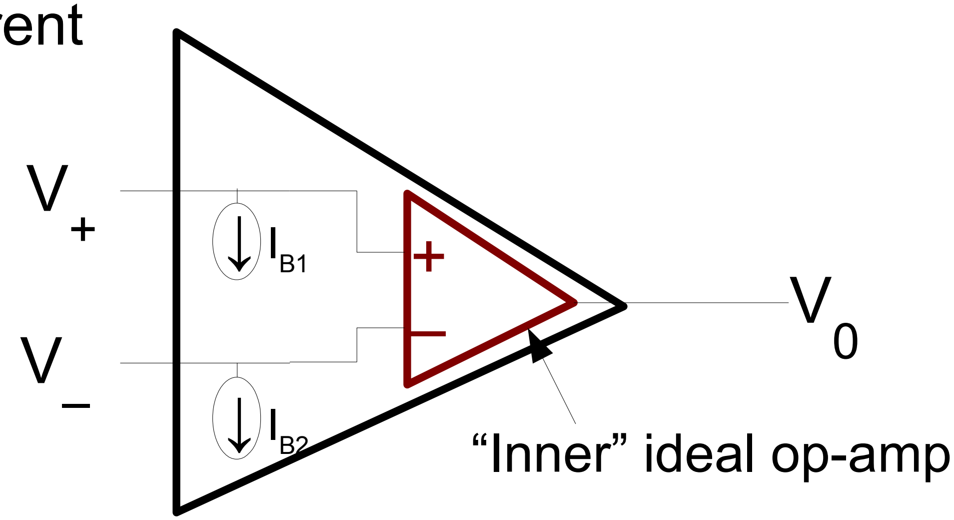


Source: www.uoguelph.ca/~antoon/gadgets

Bias Current

In a similar way to Vos, the bias current acts like an external defect to the ideal op-amp.

Input Bias Current: $I_B = ½ (I_{B1} + I_{B2})$

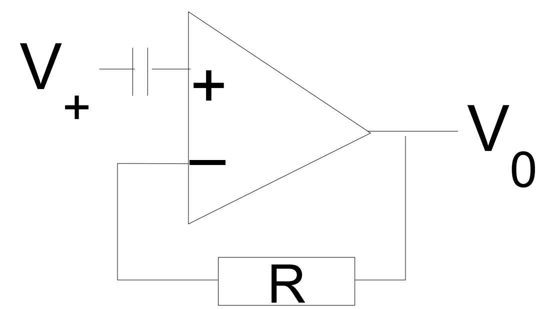


Offset voltage is larger with BJT designs + lower (almost zero with CMOS)

IB is more significant effect when gain resistors are high (V=iR)

IB drifts with time and temperature

Differential Bias current: $I_{OS} = | I_{B1} – I_{B2} |$



Consequence: you can't design a circuit without resistive path to a voltage source

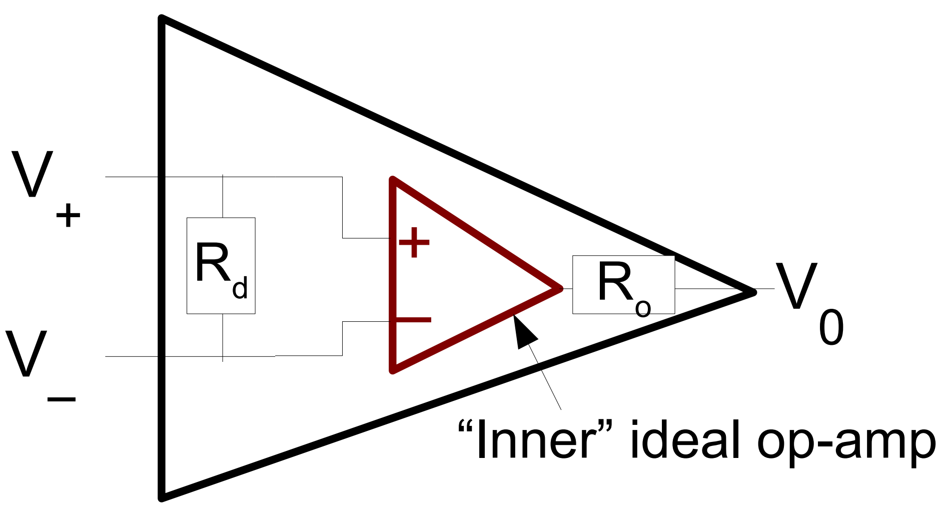
Finite Impedance Input / Output

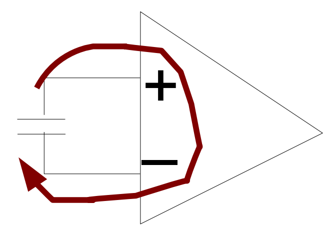
The ideal op amp has infinite input impedance (doesn't draw any current) and zero output impedance (can source to any load).

- Input Impedance: R_d
- Output Impedance: R_o

For us, the most serious is the input impedance.

- This limits the ability to not draw energy from the transducer





Current flow via non-zero input impedance

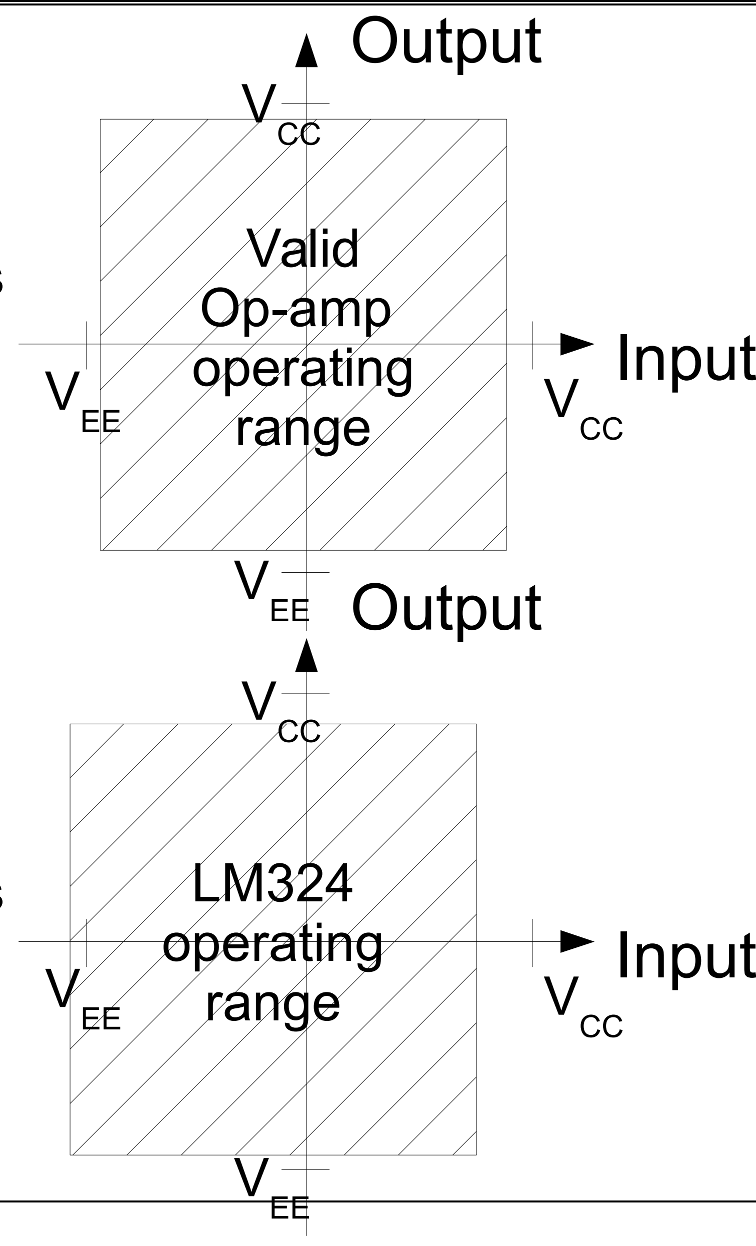
Finite Input Range

Input Range:

- The linear input range covers the inputs for which the op-amp is specified
- Generally from rail (V_{EE}) to rail (V_{CC}) less about a diode drop (0.7V)
- Special "signal supply" op amps exist (LM324) designed to go below! the negative supply (V_{EE} – 0.3V), however such designs have other compromises

Output range:

- The maximum range over which the op-amp can maintain its output
- Generally from rail (V_{EE}) to rail (V_{CC}) less about a diode drop (0.7V)



Questions: DC Imperfections

What is the CM signal? Why is it a problem?

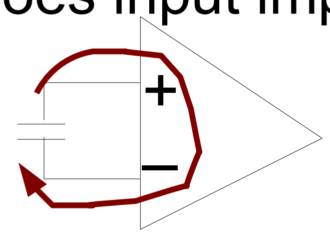
Given a difference amplifier with R3=3kΩ and R4=30kΩ. Calculate the CMRR if

- V_{OS} = 200 μV
- I_B = 10 nA
- I_{OS} = 10 nA

Name two scenarios when the PSRR can be an issue?

Considering the PSRR, how can long power leads allow noise to couple into the amplifier?

For the Piezoelectric sensor of 1pF, how does input impedance of 10GΩ affect the time constant?

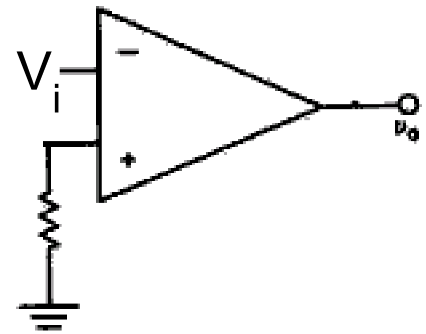


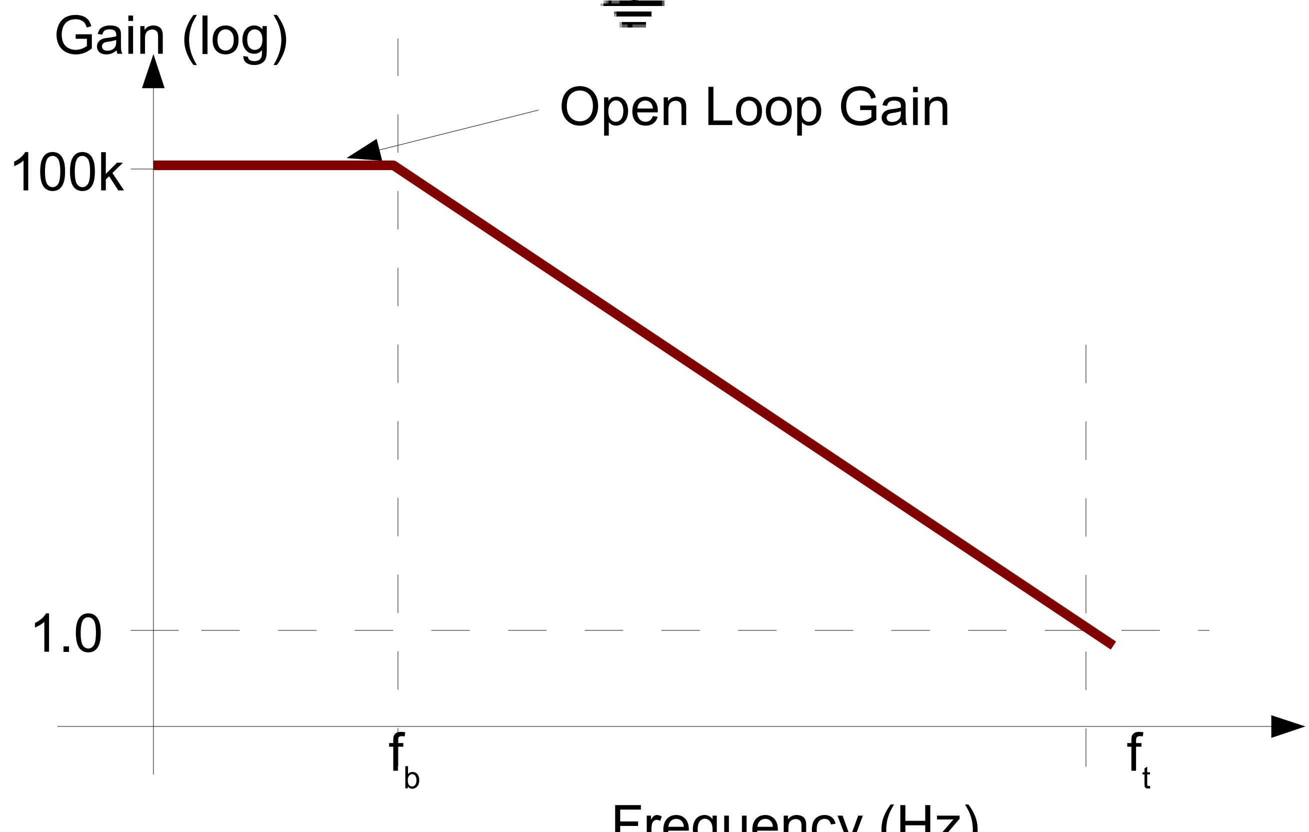
Current flow via non-zero input impedance

Gain - Bandwidth
Unity Gain Frequency

If we calculate the open loop gain:

- High gain at DC to f_b (break freq)
- Gain decreases to linearly
- Gain reaches 1.0 at f_t



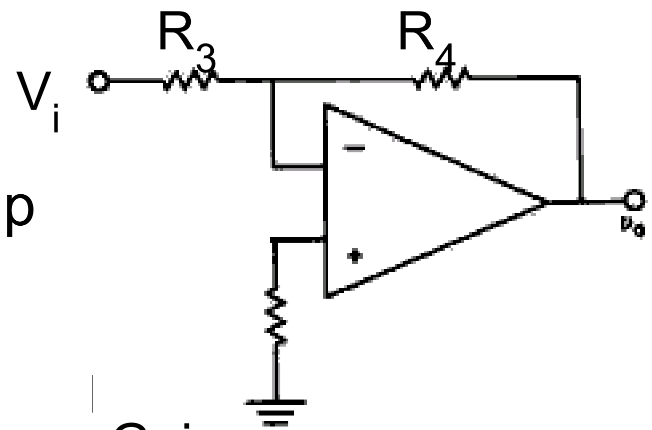


Gain-Bandwidth Limit

Closed loop Gain curve follows open-loop curve above f_t/A.

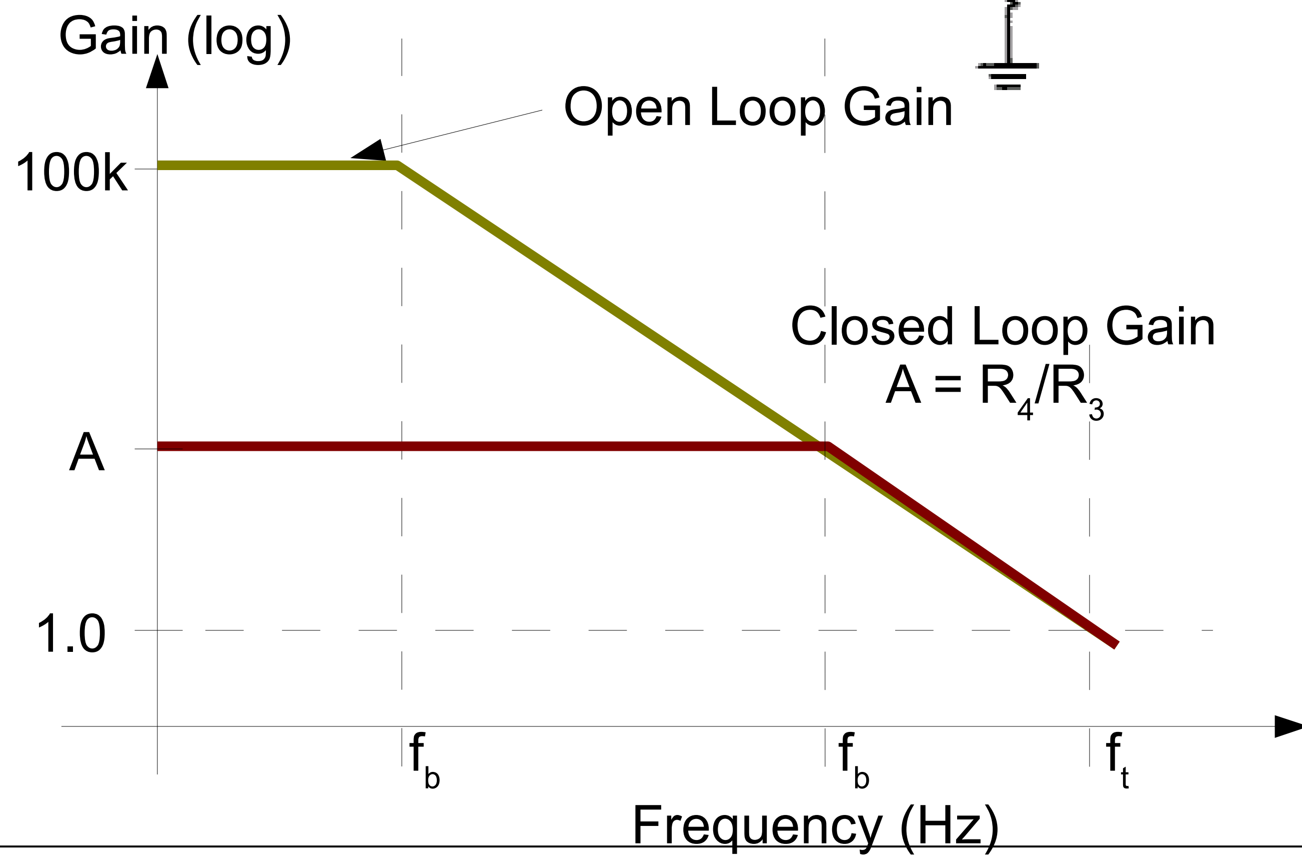
Below this curve it operates like an ideal op-amp

Therefore, don't try to get too much gain from one amplifier



$$f_b = \frac{1}{A} f_t$$

This is the gain-bandwidth limit. For a given ampli, $A \times f_b = f_t$

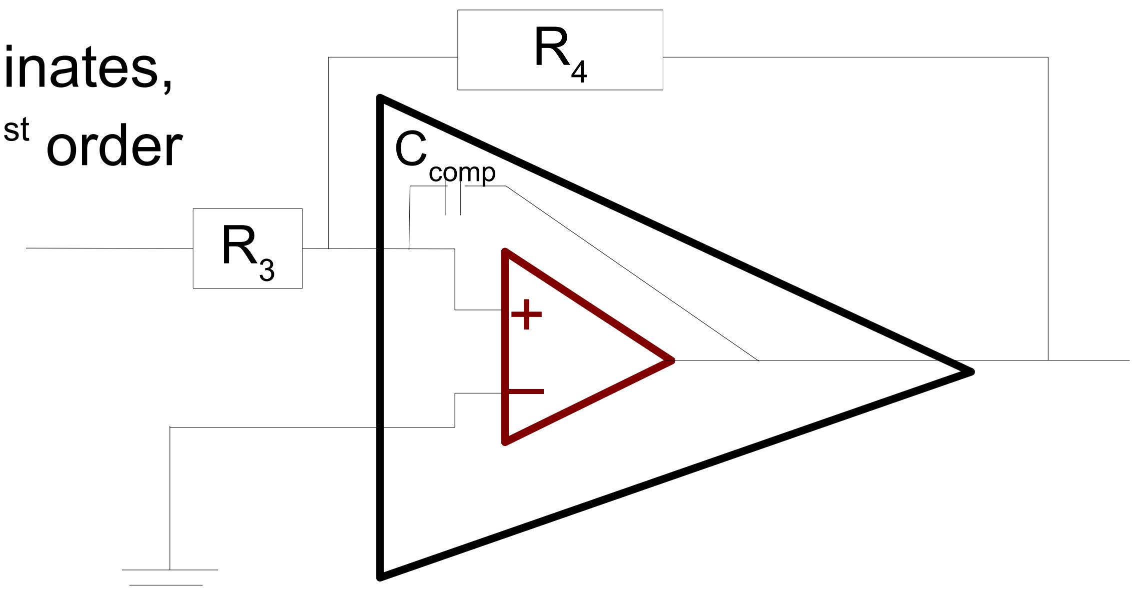


Compensated / uncompensated Op amps

The compensated op-amp has an internal capacitor to prevent oscillation.

The time const R_4C_{comp} dominates, and the gain acts like a 1st order low pass filter with

$\tau = R_4C_{comp}$



Without C_{comp}, designs need to be a lot more careful, and to provide external compensation, because op-amp will form oscillating feedback look by itself

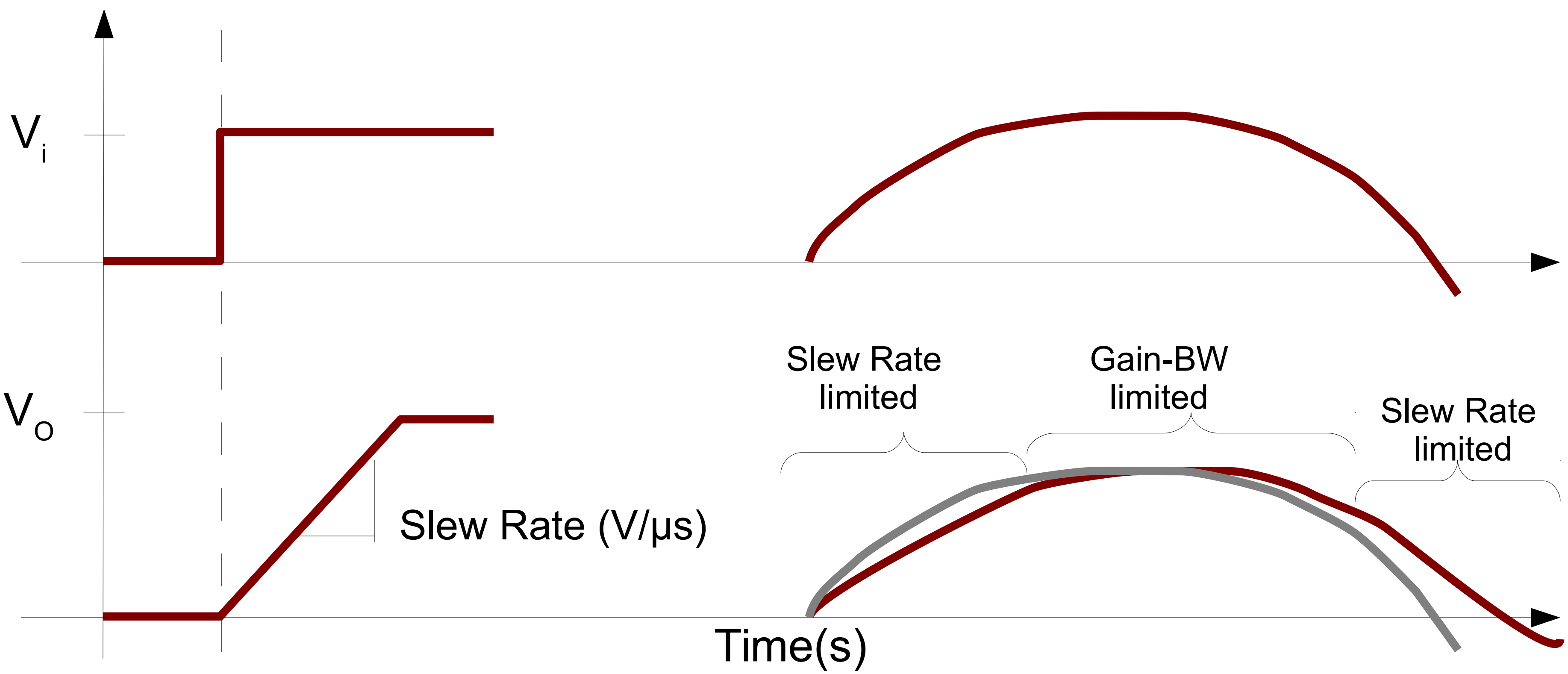
Each internal gain stage has a RC time const with a phase offset of 0 to 90°. Added together, these phase offsets make 180°, and negative feedback becomes positive.

Slew Rate

The slew rate is the maximum rate at which the output can change.

If we drive the input (V_i) with a step, the output changes as a ramp (V_o)

The slew rate imperfection dominates the large signal behaviour, while the unity gain frequency dominates the small signal behaviour.



Full Power Bandwidth

In order to test whether the signal is Slew Rate (SR) or Gain Bandwidth (GBW) limited, we calculate

$$V_i = V_{i,max} \cos(\omega t)$$
$$V_o = AV_i = AV_{i,max} \cos(\omega t)$$
$$\text{GBW limit:} \quad A(2\pi\omega) > f_t$$

$$\text{slope:} \quad \frac{dV_i}{dt} = AV_{i,max}\,\omega \sin(\omega t)$$
$$\text{max slope:} \quad AV_{i,max}\,\omega$$
$$\text{SR limit:} \quad AV_{i,max}\,\omega > SR$$

Questions: AC Imperfections

I recommend the OP07 for bioinstrumentation. However it is quite slow (0.1 V/μs). Why not choose a faster part?

A 10mV signal of 5 kHz is amplified by 100. Will an amplifier with f_t = 0.5MHz and 1 V/μs distort the output?

From a noise analysis point of view, why should we reduce BW of amplifiers?

From an EM interference point of view, why should we reduce BW of amplifiers?