SYSC3601
Microprocessor Systems

Unit 14:
Microcontrollers

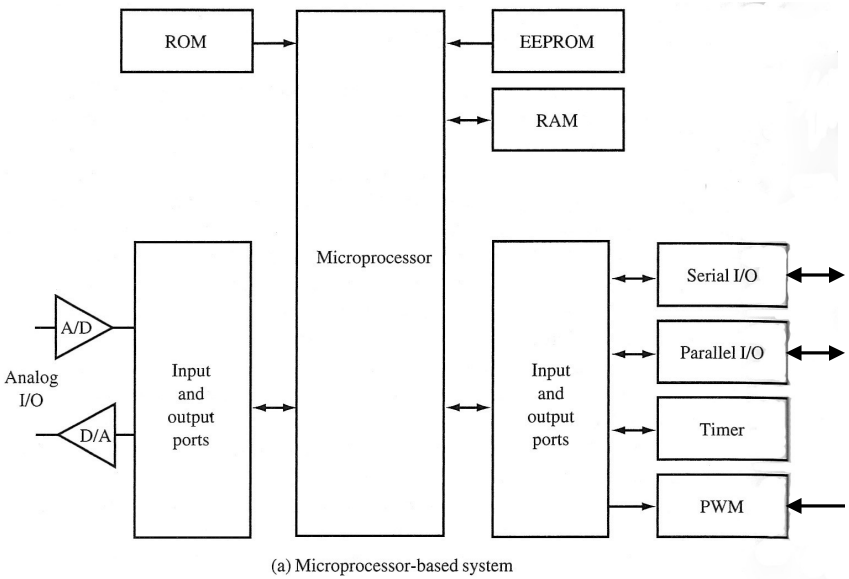
Topics/Reading

1. Microcontroller vs. microprocessor
2. MC68HC11
   - Overview
   - I/O
   - Interrupts
   - sub-systems
   - multiplexed busses
   - Motorola EVB
3. Real world applications

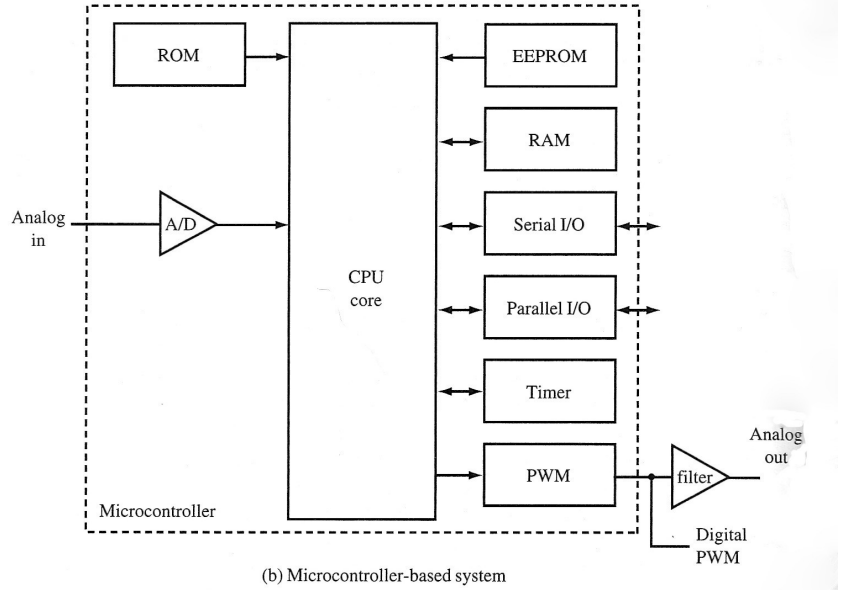
Microcontrollers

- A microcontroller is a microprocessor and more
- Chip includes many of the functions normally provided by supporting chipset
  - RAM
  - EPROM
  - Timer subsystem
  - Parallel ports
  - Serial ports
  - A/D converters
- Often used for embedded systems applications where a single chip is desirable
  - E.g. fuel injector controllers, toasters, etc.
- Pins often time-multiplexed and multi-function due to space constraints.

Microcontroller vs. Microprocessor



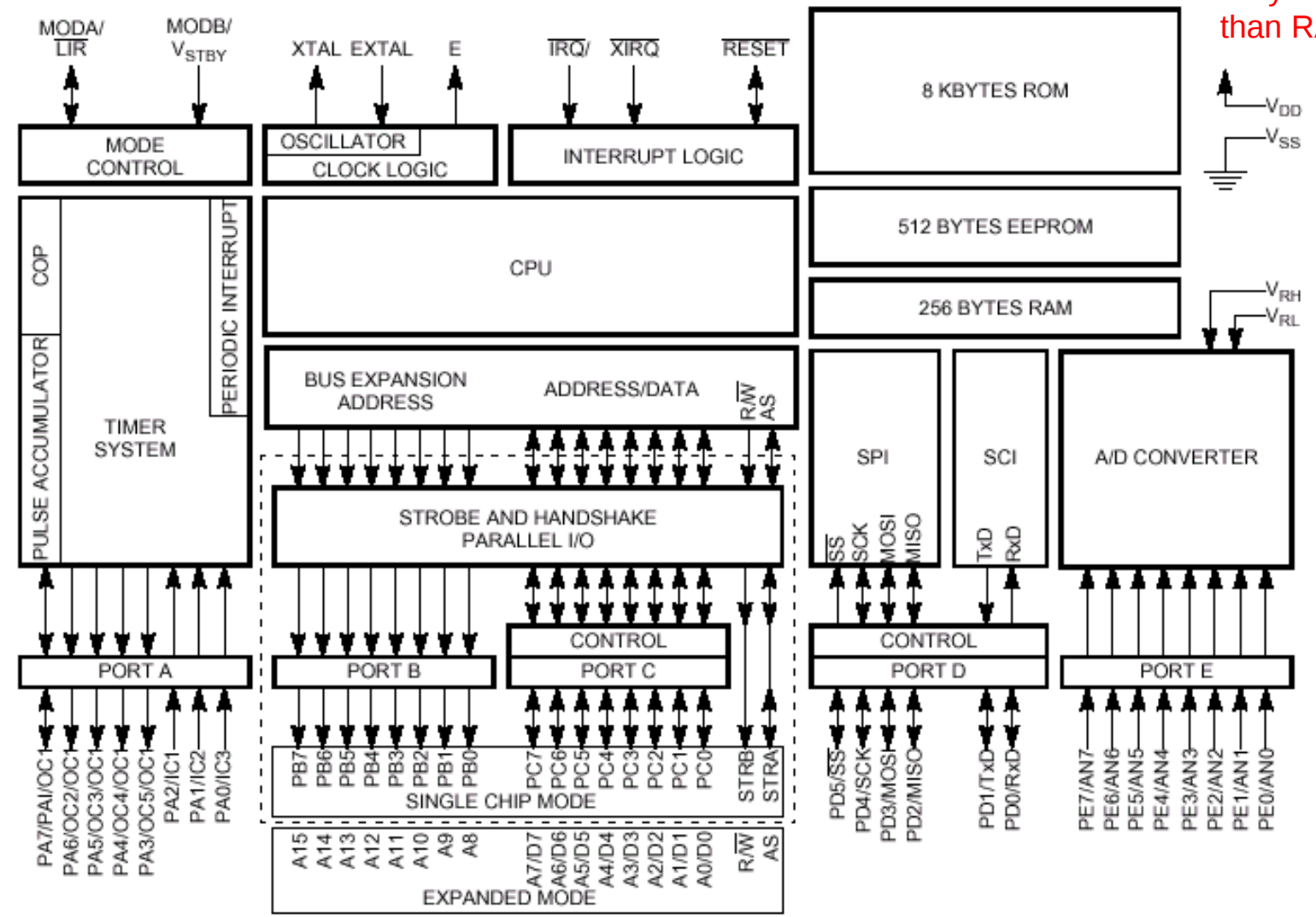
(a) Microprocessor-based system



(b) Microcontroller-based system

Microcontrollers – MC68HC11

Why more ROM than RAM?



CIRCUITRY ENCLOSED BY DOTTED LINE IS EQUIVALENT TO MC68HC24.

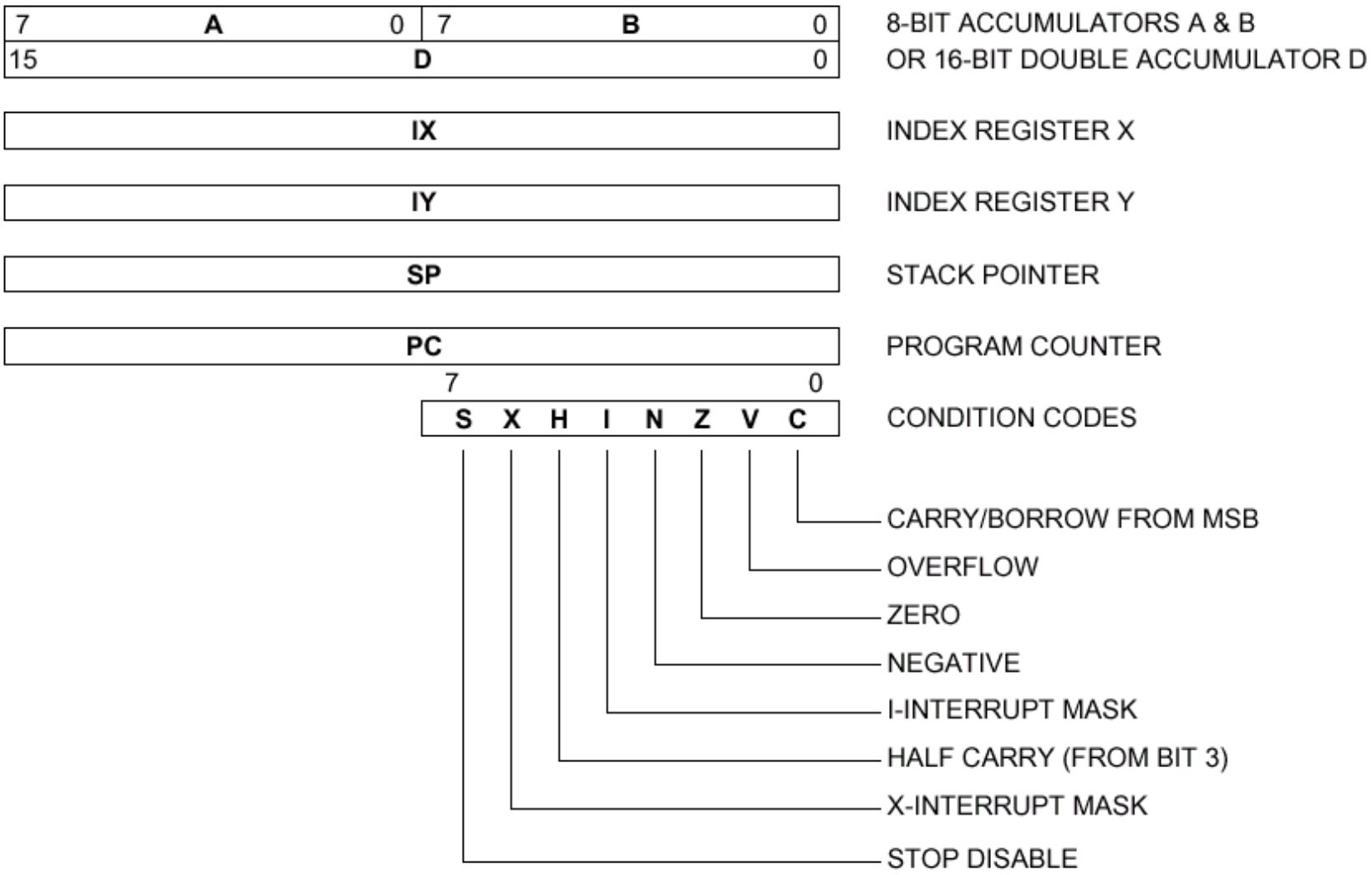
Microcontrollers – MC68HC11

- 68HC11 I/O capabilities: 68HC11 has five I/O ports with up to 38 I/O pins depending on the operating mode.

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
Port A	3	3	2	Timer
Port B	—	8	—	High-order address
Port C	—	—	8	Low-order address and data bus
Port D	—	—	6	Serial communications interface (SCI) and serial peripheral interface (SPI)
Port E	8	—	—	Analog-to-digital (A/D) converter

- PORT A: shares function with the Timer system and has 3 input-only pins, three output-only pins, and two bidirectional pins.
- PORT B: In single-chip mode, port B pins are general-purpose output only. In expanded mode, port B pins are high-order address outputs.
- PORT C: In single-chip mode, port C pins are general-purpose Input/output. In expanded mode, port C pins are multiplexed address/data bus.
  - Has a Data Direction register (DDRC) that specifies the direction of each I/O pin, a port C latched register (PORTCL), and PIOC for configuring parallel ports (handshaking/interrupts).
- PORT D: bits can be used for general-purpose I/O or with the serial communication interface (SCI) and serial peripheral interface (SPI) subsystems.
- PORT E (cont'd): is used for general-purpose input pins or shares function with the analog-to-digital (A/D) converter system.

- Programmer Model



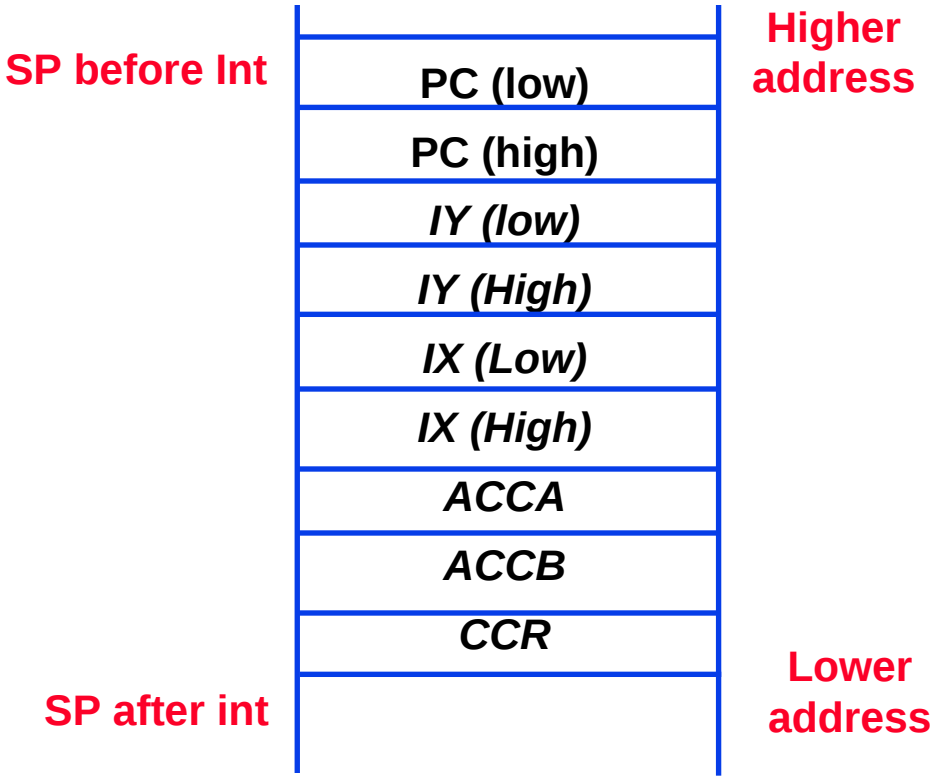
Microcontrollers – MC68HC11

- Interrupt actions in 68HC11: when an interrupt occurs the CPU automatically does the following operations:
  - The interrupt is recognized by the CPU.
  - The CPU completes the instruction it is executing.
  - The CPU pushes all registers onto the stack. It then sets the I flag bit in the CCR (disables interrupts).
  - The CPU loads the program counter with the address of the first instruction of the interrupt handler.
  - The interrupt service routine is executed.

  - The programmer (not the CPU) must insert a RTI (return from interrupt), and not RTS, as the last instruction of the ISR. This pulls all the registers off the stack, clears the flag I (enabling interrupts), and sets the PC to the instruction immediately following the instruction when the interrupt occurred.

Microcontrollers – MC68HC11

- Stack frame after an interrupt occurs in 68HC11:



- Note that RTI pulls everything off the stack when ISR is done.

Microcontrollers – MC68HC11

- How does the 68HC11 know where to find the interrupt handler?

FFC0, C1 - FFD4,D5	Reserved
FFD6, FFD7	SCI serial system
FFD8, FFD9	SPI serial transfer complete
FFDA, FFDB	Pulse accumulator input edge
FFDC, FFDD	Pulse accumulator overflow
FFDE, FFDF	Timer overflow
FFE0, FFE1	Timer input capture 4/output compare 5
FFE2, FFE3	Timer output compare 4
FFE4, FFE5	Timer output compare 3
FFE6, FFE7	Timer output compare 2
FFE8, FFE9	Timer output compare 1
FFEA, FFEB	Timer input capture 3
FFEC, FFED	Timer input capture 2
FFEE, FFEF	Timer input capture 1
FFF0, FFF1	Real-time interrupt
FFF2, FFF3	IRQ (external pin)
FFF4, FFF5	XIRQ pin
FFF6, FFF7	SWI
FFF8, FFF9	Illegal opcode trap
FFFA, FFFB	COP failure
FFFC, FFFD	Clock monitor fail
FFFE, FFFF	RESET

Sample 6811-based system

- Show slide of 68HC11 EVB
- Chips:
  - '373 for demultiplexing AD_{7-0}
  - 2K EPROM with monitor program loaded
  - 2K SRAM
  - ACIA for serial communication
    - 1488/1489 line driver/receiver for RS232
  - Reset circuit
  - 138 3-8 decoder for selecting component
  - Port Replacement Unit for parallel ports with handshaking