SYSC3601
Microprocessor Systems

Unit 8:
Direct Memory Access
(DMA)
_topics/reading

1. DMA

2. The 8237 DMA Controller

Reading: Chapter 13, sections 1-2

Direct Memory Access (DMA)

• Provides direct access to memory for I/O devices while the μP is temporarily disabled.
• Data is directly transferred between memory and the I/O device.
• Transfer rates can approach 33-150 Mbyte/s
  – Limited only by DMA Controller speed and RAM speed
  – Limited to 1.6 Mbytes/s using 8237 & 8086/88
• Used for DRAM refresh, video displays, disk read/write.
Direct Memory Access (DMA) – Basic Operation

• 2 signals are used on the µP:
  – HOLD Input used to request a DMA action
  – HLDA Output acknowledgement, transfer busses to DMA controller

• ‘DMA controller’ is essentially a special purpose µP for conducting high speed data transfers.

• During DMA transfer, the µP is effectively disconnected from the busses.

• DMA transfers data between:
  – memory ↔ I/O
  – memory ↔ memory
    • Not used in more advanced µP (faster to use CPU)
Direct Memory Access (DMA) - Sequence

1. HOLD input raised by DMA controller
2. \( \mu P \) suspends execution of its program.
   - Note that HOLD has higher priority than INTR or NMI and can interrupt instructions mid-stream (like RESET, whereas INTR/NMI wait for instruction to complete)
3. \( \mu P \) places its address, data, and control busses in high-impedance state.
4. \( \mu P \) raises HLDA to signal device that it now has complete access to the busses.
5. DMA transfer takes place.
   - On more advanced \( \mu P \), execution continues until system bus is required (from cache/pipeline)
6. Device signals \( \mu P \) that transfer is complete by dropping the HOLD signal.
7. \( \mu P \) drops HLDA.
Direct Memory Access (DMA) - Sequence

Why HLDA only after T1 or T4?

CLK

T₄ or T₁

μP input
HOLD

μP output
HLDA

DMA transfer occurs...
The 8237 DMA Controller

- A special purpose µP for conducting high speed data transfers.
- 4 DMA channels (0-3)
- Designed to manipulate the system busses in a way similar to the µP, but much faster.
  - Generates addresses and ALE
  - Generates bus control signals
    - MRDC, MWRC, IORC, IOWC
    - Note that these signals are not available on the 8086/88 in minimum mode – have to create using external circuitry.
The 8237 DMA Controller

- The µP programs the DMA controller.
  - How much data to transfer (size in bytes)
  - Where the data comes from (source)
  - Where the data goes (destination)

- Note: on the 8237, a *channel* is a path between the 8237 and the memory or I/O device.
  - Each channel includes a DREQ request line, a DACK acknowledge line, and internal registers for address, counter, configuration, etc.
  - For I/O, channel acknowledge signal bypasses address decoding and activates I/O chip directly.
The 8237 DMA Controller

• Ex: Memory-to-I/O DMA transfers
  – Only need one channel (since only 1 address).
  – I/O device requests transfer, provides source memory address
  – DACK from DMA is used to enable the I/O device (rather than decoding port address)
  – Channel selects memory address
  – MRDC and IOWC are pulled low simultaneously
  – Data is transferred from memory directly to I/O device.
The 8237 DMA Controller – Printer example

ACK from printer requests another byte (char).

DS to printer tells that new byte (char) is ready.

IOWC created by 8237 as is MRDC and mem address in this example.

JK Flip flop configured to set on falling edge of ACK

Latch selected directly via DACK₃ instead of decoding port number.
The 8237 DMA Controller

• Ex: Memory-to-memory DMA transfers
  – Channel 0: source address
  – Channel 1: destination address
  – A byte is read from address accessed by channel 0 and saved within the 8237
  – The 8237 writes the data byte to the address selected by channel 1
  – The number of bytes transferred is determined by the channel 1 count register
  – Memory-to-memory transfers are actually faster using the CPU (16-bit or 32-bit transfers…)
The 8237 DMA Controller

• Transfer Modes

1. Single Mode: release HOLD after each byte is transferred.
   - Often used when I/O can only provide 1 byte at a time (e.g. floppy disk controller) or is very slow.

2. Demand: Tx/Rx as long as DREQ is asserted.
   - Can also be interrupted by external EOP signal.

3. Batch/Block Mode: automatic Tx of a block of data until counter reaches zero.

4. Cascade: Master/Slave arrangement of more than one 8237.
Use of DMA in multi-processor environment

Local memory → Local I/O → Bus slave microprocessor → Shared Bus → Bus master microprocessor

Local memory → Local I/O → Bus slave microprocessor

Local memory → Local I/O → Bus slave microprocessor

Local memory → Local I/O → Bus slave microprocessor

Shared memory → Shared I/O