SYSC3601
Microprocessor Systems

Unit 4:
8086/88 Hardware & Bus Structure
Topics/Reading

• Brey Chapter 9: Hardware specifications
  – Pin-outs & pin functions
  – 8274 Clock generator
  – Bus buffering & latching
  – Bus timing
  – Ready & the wait state
  – Minimum mode vs. maximum mode
8086/88 Hardware and Bus Structure

• We will now focus on the 8086/88 hardware and pin functions – later we will review characteristics of other Intel µP and the Motorola family.

• Although these µP’s are fairly old, they still are a good way to introduce the Intel family of microprocessors.

• Both machines are 16-bit microprocessors. The 8088 has an 8-bit data bus and the 8086 has a 16-bit data bus.

• Still used in embedded systems (cost < $1)
Abstract diagram showing data flow in/out of $\mu$P
8086/88 Hardware and Bus Structure

• General Characteristics
  – Power:
    • 8086 +5V ± 10%, 360mA (80C86 10mA)
    • 8088 +5V ± 10%, 340mA (80C86 10mA)
  – Temp:
    • 32ºF - 180ºF (not suitable for outdoors)
    • CMOS version -40ºF - 255ºF (MIL spec)
  – Clock Frequency:
    • normally 5MHz. SDK86: 2.5MHz or 5MHz.
  – DC characteristics
    • Must understand V-A characteristics of I/O pins in order to connect to the outside world. (next slide)
Input characteristics

• compatible with standard logic-level components
  – logic 0: 0.8V max, 10μA max
  – logic 1: 2.0V min, 10μA max
• The input current is very small – gates of MOSFETs, so current represents leakage.

Output characteristics

• logic 1 voltage level is compatible with most logic families, but logic 0 is not. (Most logic families have logic 0 max 0.4V)
  – logic 0: 0.45V max, ± 2.0 mA max
  – logic 1: 2.0V min, ± 400 μA max
• No more than 10 loads per output without buffering.
• If more than 10 loads are attached to any bus pin, then the entire 8086/8088 must be buffered.
### 8086/8088 Pin Assignments & Functions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vcc</td>
<td>40</td>
<td>Vcc</td>
</tr>
<tr>
<td>2</td>
<td>A14</td>
<td>39</td>
<td>A15</td>
</tr>
<tr>
<td>3</td>
<td>A13</td>
<td>38</td>
<td>A16/S3</td>
</tr>
<tr>
<td>4</td>
<td>A12</td>
<td>37</td>
<td>A17/S4</td>
</tr>
<tr>
<td>5</td>
<td>A11</td>
<td>36</td>
<td>A18/S5</td>
</tr>
<tr>
<td>6</td>
<td>A10</td>
<td>35</td>
<td>A19/S6</td>
</tr>
<tr>
<td>7</td>
<td>A9</td>
<td>34</td>
<td>SS0</td>
</tr>
<tr>
<td>8</td>
<td>A8</td>
<td>33</td>
<td>MN/MX</td>
</tr>
<tr>
<td>9</td>
<td>RD</td>
<td>32</td>
<td>MN/MX</td>
</tr>
<tr>
<td>10</td>
<td>HOLD</td>
<td>31</td>
<td>HOLD</td>
</tr>
<tr>
<td>11</td>
<td>HLDA</td>
<td>30</td>
<td>HLDA</td>
</tr>
<tr>
<td>12</td>
<td>WR</td>
<td>29</td>
<td>WR</td>
</tr>
<tr>
<td>13</td>
<td>M/IO</td>
<td>28</td>
<td>M/IO</td>
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<tr>
<td>14</td>
<td>DT/R</td>
<td>27</td>
<td>DT/R</td>
</tr>
<tr>
<td>15</td>
<td>DEN</td>
<td>26</td>
<td>DEN</td>
</tr>
<tr>
<td>16</td>
<td>ALE</td>
<td>25</td>
<td>ALE</td>
</tr>
<tr>
<td>17</td>
<td>NMI</td>
<td>24</td>
<td>INTA</td>
</tr>
<tr>
<td>18</td>
<td>INTR</td>
<td>23</td>
<td>TEST</td>
</tr>
<tr>
<td>19</td>
<td>CLK</td>
<td>22</td>
<td>READY</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>21</td>
<td>RESET</td>
</tr>
</tbody>
</table>

8086/8088 DIP pin assignments (max mode in brackets)
Both the 8086 and the 8088 are 40-pin Dual In-line Package (DIP) chips.

- 8086 – 16-bit µP and a 16-bit data bus
- 8088 – 16-bit µP and a 8-bit data bus
- 8086 has M/IO, 8088 has IO/M
  - See text Fig 9-1. Note that on 8088, IO/M should be IO/M
- Pin 34 is also different: 8086 BHE/S7, 8088 has SSO
8086/8088 Pin assignments & functions

- **AD\textsubscript{15} - AD\textsubscript{0}**
  - Multiplexed address/data bus.
  - lines carry address bits A\textsubscript{15} - A\textsubscript{0} whenever ALE (Address Latch Enable) is logic 1.
  - lines carry data bits D\textsubscript{15} - D\textsubscript{0} whenever ALE is logic 0.
  - Note: 8088 only multiplexes D\textsubscript{7} - D\textsubscript{0} because it uses an 8-bit data bus.

- **A\textsubscript{19}/S\textsubscript{6} - A\textsubscript{16}/S\textsubscript{3}**
  - multiplexed address/status bits.
  - lines carry address bits A\textsubscript{19} - A\textsubscript{16} whenever ALE is logic 1.
  - lines carry status bits S\textsubscript{6} - S\textsubscript{3} whenever ALE is logic 0.
8086/8088 Pin assignments & functions

- \( S_6 \) always logic zero (not used).
- \( S_5 \) matches state of I flag bit (interrupt)
- \( S_4 \& S_3 \) reports segment being accessed during current bus cycle:

<table>
<thead>
<tr>
<th>( S_4 )</th>
<th>( S_3 )</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Extra Segment (ES)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Stack Segment (SS)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Code Segment (CS)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Data Segment (DS)</td>
</tr>
</tbody>
</table>

- Note: These status lines could be decoded/latched to address four separate 1M banks of memory. (Split I/D)
8086/8088 Pin assignments & functions

- **RD** µP is set to receive data when low
- **WR** µP is outputting data when low
- **M/IO** (8086) indicates a memory address (‘1’), or an I/O address (‘0’).
- **DT/R** Data transmit/receive. Data bus is transmitting (‘1’), or receiving (‘0’) (for controlling bi-directional bus drivers).
- **DEN** Data bus enable – used to activate external buffers/transceivers.
- **BHE/S7** Bank high enable
  - used to enable D_{15} - D_{8} in an 8086 during a 16-bit read/write.
  - Multiplexed with S7, which is not used (always 1).
  - latched with ALE.
8086/8088 Pin assignments & functions

- **READY**: Used to insert wait states (controlled by memory and IO for reads/writes) into the microprocessor.

- **RESET**: Microprocessor resets if this pin is held high for 4 clock periods. Instruction execution begins at FFFF0H and IF flag is cleared.

- **CLK**: Provides clock signal to 8086

- **HOLD**: Requests a direct memory access (DMA). When 1, microprocessor stops and places address, data and control bus in high-impedance state.

- **HLDA** (Hold Acknowledge): Indicates that the microprocessor has entered the hold state.

- **RO/GT<sub>1</sub> and RO/GT<sub>0</sub>**: Request/grant pins request/grant direct memory accesses (DMA) during maximum mode operation.
8086/8088 Pin assignments & functions

- Pins to be discussed later:
  - **INTR**: Used to request an interrupt
  - **NMI**: Used to request a non-maskable interrupt
  - **INTA**: Output to acknowledge an interrupt.
  - **TEST**: An input that is tested by the WAIT instruction. Commonly connected to the 8087 coprocessor.
  - **QS_1** and **QS_0**: The queue status bits show status of internal instruction queue. Provided for access by the numeric coprocessor (8087).
  - **LOCK**: Lock output is used to lock peripherals off the system. Activated by using the LOCK: prefix on any instruction.
8086/8088 Pin assignments & functions

• Both the 8086 and the 8088 have two modes of operation:
  1. Minimum Mode: connect MN/MX to +5V (directly).
     – similar to 8085 operation.
     – all control signals for memory and I/O are generated by the µP.
     – (RD, M/IO, DT/R, DEN, ALE, INTA, WR, etc)
  2. Maximum Mode: connect MN/MX to ground (directly).
     – dropped by Intel beginning with the 80286.
     – must use with co-processor (8087) present.
     – some control signals must be generated externally.
     – use with 8288 bus controller.
8288 Bus Controller *(use when in MAX mode)*

8288 Bus Controller
\[ s_{0-3} = \text{state data from 8086} \]

8282 Tri-State Octal Latch
- \( \text{STB} = \text{data strobe (admit new data)} \)
- \( \overline{\text{OE}} = \text{output enable} \)

8286 Octal Bus Transceiver
- \( T = \text{transmit} \)
- \( \overline{\text{OE}} = \text{output enable (in either dir)} \)

Some details omitted…
We will see how to achieve buffering & demultiplexing using generic chips…
Decoding Bus Control Signal

• In “max mode” use 8288 bus controller to generate MRDC, MWTC, IORC, IOWC.
• In “min mode” (and for other processors) it is sometimes better to decode the available signals.
8284A Clock Generator

- Used with 8086/88 to generate
  1. clock signal (see next slide)
  2. reset signal (see next slide)
  3. ready signals (wait states)

- Inputs:
  - $F/\bar{C}$ Frequency/crystal select.
    1 $\rightarrow$ external clock
    0 $\rightarrow$ crystal ($X_1\text{-}X_2$ provides timing).
  - CSYNC Only used with external clock, otherwise grounded.
  - RES Reset input pin. Generates RESET output.
8284A Clock Generator

10K pullup? 0.5mA sink. (debouncing!)
Bus Transfer Synchronization

- Synchronous busses (eg. Motorola 6800/11/12)
  - Transfer times and synchronization are tied to the system clock.
  - No facility for varying bus timing.
  - Clock generators could be used to vary bus speed (for slower memory), but would slow entire µP

- Semi-synchronous busses
  - provide for “wait states” to be inserted into bus timing (eg. 8086).
  - Allows more flexibility in interfacing to slower memory or I/O.

- Asynchronous busses (eg. Motorola 68000)
  - Requires extra bus signals for bus arbitration.
  - Requires “acknowlegement” signal from devices.
  - Requires bus time-out (watchdog).
  - Easier multiprocessor memory management.
Bus Timing

• 8086 and 8088 bus cycles consume four system clock periods (T-states), $T_1$, $T_2$, $T_3$ and $T_4$.

• At 5MHz, each T-state is 200nS, therefore a bus cycle is 800nS.

• Semi-synchronous bus control allows inserting of wait states ($T_w$), also 200nS, between $T_3$ and $T_4$ which allows access to slow memory and I/O devices
  – (Text says $T_w$ inserted between $T_2$ and $T_3$, but the Intel manual says between $T_3$ and $T_4$).

• Most processors are very similar in I/O and memory access operations.
Write Cycle
Read Cycle

ONE BUS CYCLE

T₁  T₂  T₃  T₄

CLK

ADDRESS /DATA

address

data (TO µP)

ALE

RD
Read/Write Cycle Events

- $T_1$: Address, ALE, DT/R, M/IO.
- $T_2$: RD, WR, DEN, data on the bus (for write).
- At the end of $T_2$ (middle of $T_3$), µP samples READY.
  - (a) while READY = 0; do
  - (b) insert $T_w$.
- $T_3$/$T_w$: Gives time for memory or I/O device to read/write.
- For read cycles, data bus is sampled at end of $T_3$.
- $T_4$: All bus signals are deactivated.
- Normal memory access time is 460nS. Slower devices will need at least one wait state which will give 660nS.
Wait State Generation using 8284A

8-bit shift register will generate 1 wait state high until read/write from mem

CS from memory devices will generate 1 wait state

8-bit shift register

15MHz

Vcc

10k

10µF

X1 RDY1

÷ 3

X2

8284A

READY

RES CLK

RESET

8086

8284A

74LS164

CLR

SI

Vcc

READY

RESET

CLK

RD

WR

INTA
Example Timing for 2 Wait States

[Diagram showing timing of signals such as Clock, A/D, RD, CLR, Shift Reg, QA, QB, QC, CS, RDY1, READY, Check READY, with timing intervals T1, T2, T3, TW1, TW2, T4 marked.]
Bus Latching and Buffering

- Latches are used to de-multiplex the address/data and address/status lines and commonly have output buffers for driving external loads.
- Buffers are used to drive external loads, and to isolate component when disabled.

<table>
<thead>
<tr>
<th>D</th>
<th>Q</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
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OE

74LS373 Octal Latch

<table>
<thead>
<tr>
<th>IN</th>
<th>OUT</th>
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<tbody>
<tr>
<td>0</td>
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<td>1</td>
<td>1</td>
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OE

74LS244 Octal 3-State Buffer

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Dir</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td></td>
</tr>
<tr>
<td>1</td>
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</table>

G (or OE)

74LS245 Bus Transceiver

<table>
<thead>
<tr>
<th>D</th>
<th>Q</th>
<th>STB</th>
</tr>
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<tbody>
<tr>
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<td></td>
</tr>
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OE

8282 Tri-state Octal Latch

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
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<tbody>
<tr>
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</tr>
<tr>
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<td>7</td>
</tr>
</tbody>
</table>

OE

8286 Tri-state Octal Bus Transceiver
Three-state Buffer (Tri-state buffer)

- When enabled by the control line, output follows input (buffered, pass-through).
- When disabled, output is a very high impedance which prevents the output from driving or loading connected circuits.
- When disabled, the outputs are said to be floating.
- In effect, it is like a switch.
Bidirectional buffers (transceivers)

<table>
<thead>
<tr>
<th>DIR</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>B → A</td>
</tr>
<tr>
<td>1</td>
<td>A → B</td>
</tr>
</tbody>
</table>

EX: 74LS245 octal bus transceiver.
Latches (D-type flip-flops)

- When enable is high, Q follows D.
- When enable goes low, Q maintains (latches) state of D.
- Eg:
  - 74LS373 (latched on falling edge).
  - 74LS374 (latched on rising edge)