Carleton University

Dept. of Systems and Computer Engineering

Microprocessor Systems—SYSC 3601 Summer 2014

Course Outline

Instructor Dr. Ramy Gohary, Office: ME4474, T. 613-520-2600 Ext. 1579, Email: `gohary@sce.carleton.ca`, Office hours: Monday and Friday 1:30–3:00.

TA Mr. Mohamed Aslan, Office: ME 4463, Email:`MohamedAslan@cmail.carleton.ca`.

Course Objectives To familiarize students with microprocessor-based circuit design. The course deals with the applications, organization, architecture, and design of microprocessor systems. Topics covered include addressing, bus structures, memory and I/O interfacing, interrupt mechanisms, and related techniques at the hardware and assembly language levels.

Prerequisites ELEC2607 and SYSC2003 or Permission of the Department (request permission using the online form at www.sce.carleton.ca/ughelp). Students must satisfy the prerequisites in order to remain registered in the course. Students who have not completed the prerequisites are required to withdraw from the course or they may be deregistered from the course after the last day for course registration. Precludes additional credit for SYSC 3501 or SYSC 4600.

Lectures: Two three-hour lectures per week.

Laboratory: Three hours per week.

Instructional Resources Lectures: Tuesday and Thursday, 1:00 am–4:00 pm in 3165 ME.
Labs: Tuesday and Thursday 10:00 am–1:00 pm in 4135 ME. The first week of labs will be announced in the lectures.
Website: `http://www.sce.carleton.ca/courses/sysc-3601/s14/`—Please check the website regularly; important announcements will be posted there as the course progresses.
TA: Mr. Mohamed Aslan will supervise and mark the labs. For help with the labs, you can arrange with Mr. Aslan by email: `MohamedAslan@cmail.carleton.ca`.
Instructor: I will be available during my scheduled office hours. You can also reach me by email to schedule an appointment.

Textbooks

- Barry B. Brey, "The Intel Microprocessors: 8086/8088, 80186, 80286, 80386, 80486, Pentium, Pentium Pro Processor, Pentium II, Pentium III, Pentium 4 Architecture, Programming, and Interfacing," Fourth, Fifth, Sixth, Seventh or Eighth Edition.
- J.L Antonakos, The 68000 Microprocessor, Prentice Hall, QA76.8.M6895A57, ISBN 0-13-668120-4.

Laboratories There will be four laboratory exercises. Each exercise requires the completion of a pre-lab component. Lab manuals will be posted on the course website a week before each lab. The TA will discuss and assess your work in the lab. Late reports will not be accepted.
Lab exemptions will not be granted for this course, and attendance at the scheduled laboratory periods is mandatory. If you are unable to attend a lab due to medical reasons, you must provide a medical note within one week of returning to campus.

Students without the prerequisites or a prerequisite waiver will be deregestired from the course after the last day to register for courses in the Summer 2014 term.

Examinations There will be a mid-term exam and a written final exam. Both exams will be closed-book. The mid-term will be held during the lecture of Tuesday, July 29, 2014. The final exam will be held during the University's examination period in August. The final exam is for evaluation purposes only and will not be returned to students.

The "Academic Regulations of the University" permit instructors to specify requirements that must be satisfied for students to be eligible to write the final examination or, where circumstances warrant, apply to the Registrar's Office for deferral of the final examination.

- All students are encouraged to write the final examination.
- Students who miss the final exam, but completed all labs, and attempted the mid-term exam, will receive the grade ABS. These students are eligible to apply for deferral of the final examination. For more information, see the current Undergraduate Calendar, Academic Regulations of the University, Section 2.2, The course Outline; Section 2.3, Standing in Courses/Grading System; and Section 2.5, Deferred Final Examinations.
- Students who miss the final exam, and did not complete all labs or missed the mid-term exam, will receive the grade FND. These students are ineligible to write the deferred final exam.

In-class participation Students will be expected to participate in in-class discussions and to write 5-minute quizzes.

Grading Scheme

- Lab work: 15%
- In-class participation and quizzes: 15%
- Mid-term Exam: 25%
- Final Exam: 45%

Attendance Students are expected to attend all lectures and lab periods. The Faculty of Engineering and Design requires its students to have a conflict-free timetable. Hence, requests to accommodate missed exams, assignment due dates, etc., because of conflicts with other courses, jobs or vacation plans will not be considered.

Students with Disabilities Students with disabilities requiring academic accommodations in this course should contact the Paul Menton Centre for Students with Disabilities (PMC) (UC 500) to complete the necessary forms. After registering with the PMC, make an appointment with your instructor to discuss your specific needs at least two weeks prior to the mid-term exam. This will allow sufficient time to make the required arrangements.

Academic accommodation for religious obligations Students who require accommodations due to religious obligations must follow the procedures described in Section 2.10 of the "Academic Regulations of the University".

Health and Safety Every student should have a copy of our Health and Safety Manual. An electronic version of the manual can be found at `http://www.sce.carleton.ca/courses/health-and-safety.pdf`.

List of topics to be covered in the lectures

- Background and Introduction
  - Microprocessor history, types, applications and selection
  - General microprocessor architecture
  - Review of number systems
  - Intel and Motorola microprocessor families
- The Intel 80X86/88 Architectures and Programming
  - Registers and Internal Architecture
  - Address generation and addressing modes
  - Instruction set and assembly language programming
  - The SDK-86 System Development Kit
- The Intel 80X86/88 Bus and Buffering
  - 80X86/88 Pin functions, states, bus cycles and signalling waveforms
  - Clock generators (Intel 8284) and bus controllers (Intel 8288)
  - Latches (74373) and bus transceivers (74245)
  - Wait states and bus timing
- Memory Structures and Interfacing
  - Memory types and characteristics (DRAMs, SRAMs, ROMs, EPROMs)
  - Address decoding
  - Memory interfacing
- Input/Output Systems (I/O)
  - Programmed I/O structures
  - I/O ports design and address decoding
  - Programmable Peripheral Interface Chips (Intel 8255A)
  - Keyboard/Display Interface (8279)
- Interrupt Systems
  - Interrupt Types (HW, SW and Exceptions)
  - Interrupt structures
  - Programmable Interrupt Controllers (Intel 8259 PIC)
  - Programmable Counters/Timers (8253)
- Direct Memory Access

  - Introduction to DMA structures
  - Intel 8237 DMA Controller
- Motorola 680X0 Microprocessor Architecture
  - Basic architecture and register structure
  - Address generation and addressing modes
  - Assembly language programming
- Motorola Memory and I/O Structures
  - Memory organization and interfacing
  - I/O interfacing
  - Interrupt and exception vectors and INTA Cycle
  - Vectored and autovectored interrupts
- Floating Point Coprocessors
  - Co-processor architecture (Motorola or Intel)
  - Coprocessor programming and interfacing
- Serial Communications and Other Interfacing Chips
  - Synchronous vs. asynchronous communications
  - Programmable communication interfaces (Intel 8251A USART)
- Other Microprocessors and Bus Structures
  - Intel Pentium and Pentium Pro microprocessors
  - Motorola 68020, 68030, 68040, and 68060 microprocessors
  - Motorola 68HC11 Microcontroller family
  - System buses (ISA, PCI, VME)
- Miscellaneous Topics and Review
  - Microcontrollers
  - RISC vs. CISC architectures
  - Introduction to DSPs
