Carleton University

Dept. of Systems and Computer Engineering

Microprocessor Systems—SYSC 3601 Mid Term Exam

Instructor: Dr. Ramy Gohary

July 29, 2014

Instructions:

1. No calculators, notes, or books allowed.
2. All questions are to be answered on the examination booklet provided.
3. The total mark is 125 points—25 bonus points.
4. Time allowed 2 hours, unless otherwise instructed.

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1. Introduction and overview on microprocessor systems: 20 marks total
   (a) Sketch, list and explain the functionality of the components of the Von Neumann model. 5 marks
   (b) To which component in the Von Neumann model do the following entities belong: flash memory, DVD-RW, ROM, hard disk, microprocessor? 5 marks
   (c) How many bytes are there in a 4G $\times$ 8 memory section? How many bits are needed to address each location in this section? 5 marks
   (d) The double-word AC43BCBCH is stored in the memory location starting at A0000H of an 8088-based microprocessor system. Draw a memory map indicating the exact location of eah byte of this double-word. 5 marks

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2. Programming model 25 marks total
   (a) Give an example of three instructions, each one automatically affects one of the following: CX, SP and the Z flag. 5 marks
   (b) Suppose that DS=1000H, SS= 2000H, CS=3000H, ES=4000H, BP=FFH, BX=FFFFH and DI=5H.
      i. Which memory locations are addressed by: MOV DL, [BP]? 2.5 marks
      ii. Which memory locations are addressed by: MOV EAX, [BX+DI]? 2.5 marks
   (c) Explain why the max size of a memory segment in the real addressing mode is 64K. 5 marks
   (d) Code a descriptor that describes a data memory segment that grows upward and begins at location 03000000H and ends at location 05FFFFFFH and can be written. The memory has not been accessed, and can be accessed with the lowest privilege level. Assume that the segement is available (i.e., AV=1) and that the instructions are 32 bits (i.e., D=1). 10 marks

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3. Addressing modes and machine coding 25 marks total
   (a) Machine encode the instruction: MOV AX, [BX+DI+2H]. 5 marks
   (b) What is the instruction corresponding to the following machine code: 8CC8H? 5 marks

(c) Let IP=0100H and CS=1000H before executing the previous instruction. What are the contents of the memory location CS:IP and CS:IP+1? 5 marks

(d) Estimate the execution time of the following code: 10 marks

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        MOV DI, FH
Again:  ADD [1234H+DI],AL
        DEC DI
        JNZ Again
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4. The 8086 and 8088 hardware and bus structure 25 marks total

(a) Suppose that a microprocessor operates at 5MHz. How long does the bus cycle occupy, assuming no wait states are inserted? 5 marks

(b) What happens during T_1, T_2, T_3 and T_4 of a standard write bus cycle? Show a timing diagram. 10 marks

(c) Design a circuit that uses the 8284A clock generator and an 8-bit shift register to insert two wait state in the bus cycle of the 8086 microprocessor. Don't forget to show the signal coming from the external device that needs the wait states. 10 marks

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5. Memory interfacing: Design a memory interface for the 80886 which will provide 128K bytes of SRAM, organized as 64K×16 bits, starting at address 50000H and using 62256 SRAM 32K×8 chips. Follow the following steps to arrive at the required design. 30 marks total

(a) How many chips are required? 3 marks

(b) How man address lines go to each chip? 2 marks

(c) How will the chips be organized in banks? Which parts of the address bus will be used? 5 marks

(d) Determine the address range. 5 marks

(e) Generate the overall chip select signal. 5 marks

(f) Generate bank-specific write signals. 5 marks

(g) Connect the address bus, the data bus and the control signals: $\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, $M/\overline{IO}$ and $\overline{BLE}$. 5 marks

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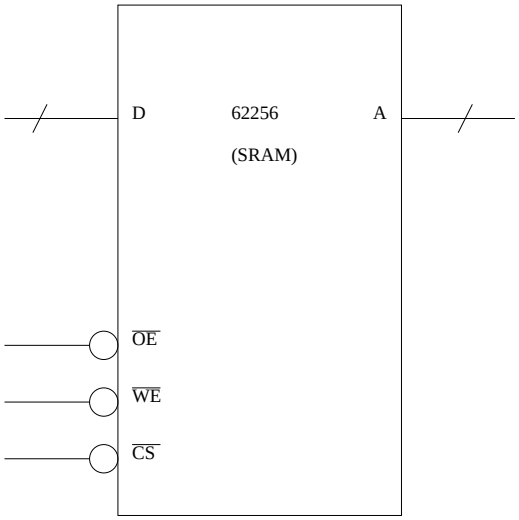
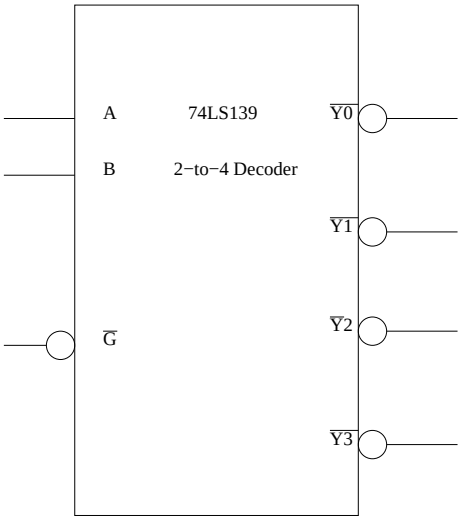
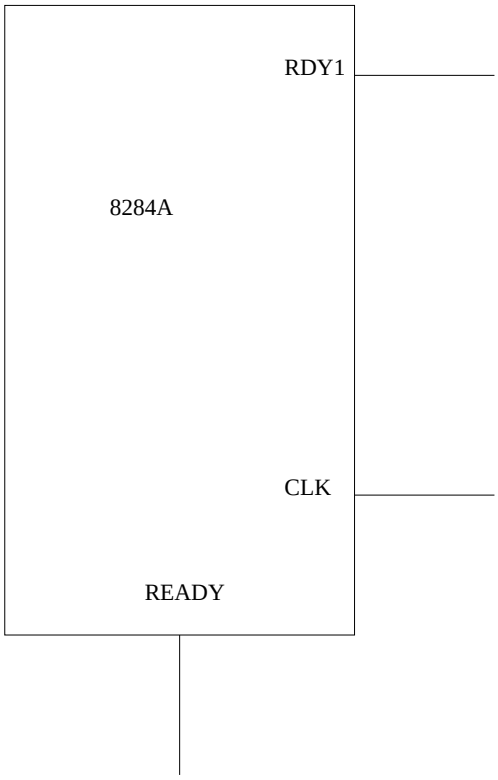
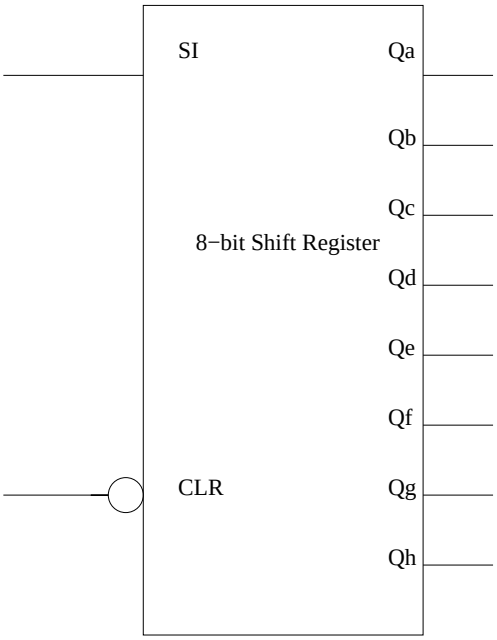
Good luck!

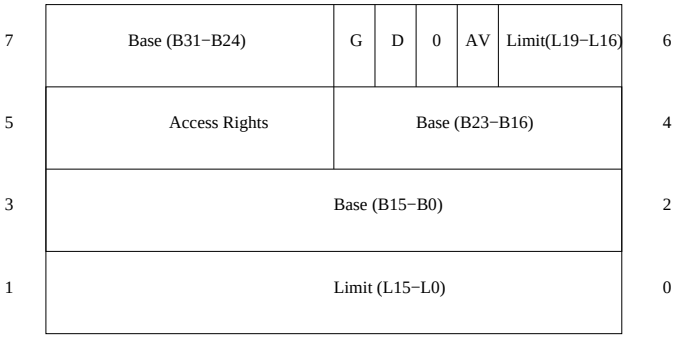

D
62256
(SRAM)
A
OE
WE
CS


A
74LS139
B
2−to−4 Decoder
G
Y0
Y1
Y2
Y3

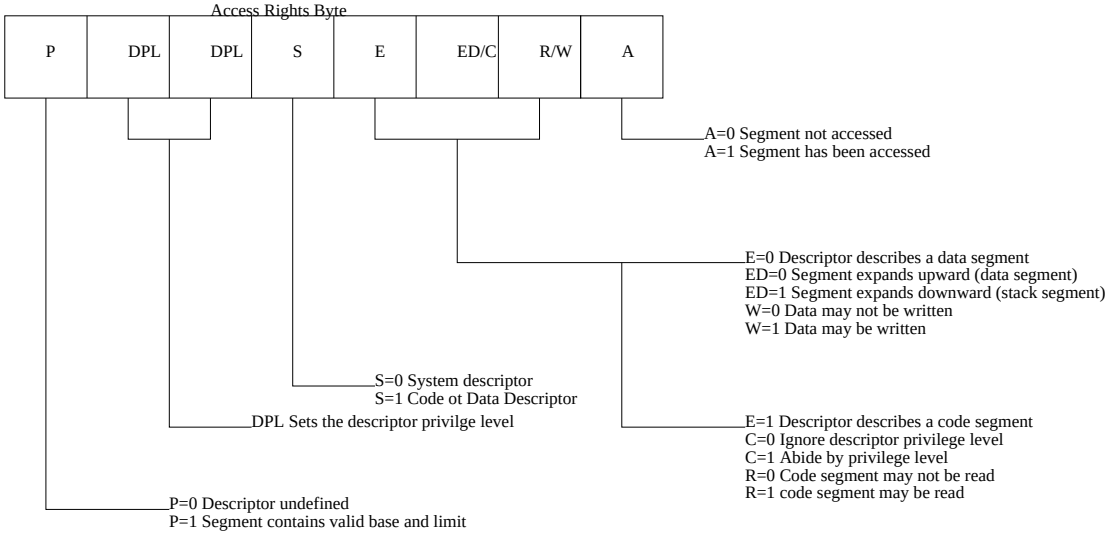

RDY1
8284A
CLK
READY


SI
Qa
Qb
Qc
8−bit Shift Register
Qd
Qe
Qf
CLR
Qg
Qh

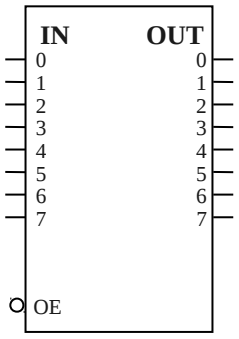
80386 through Pentium 4 Descriptor



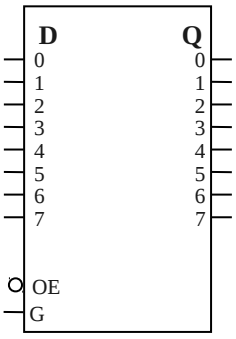
Access Rights Byte



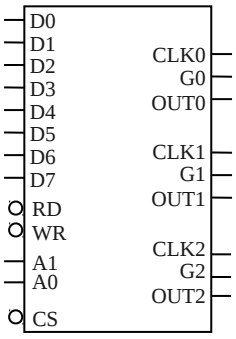
Toolbox



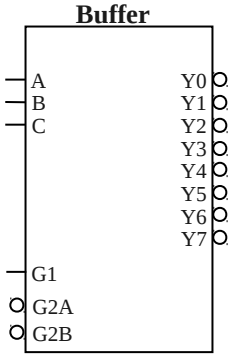
74LS244
Octal 3-State Buffer
Buffer



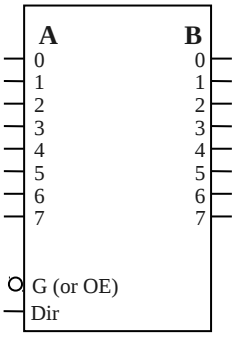
74LS373
Octal Latch



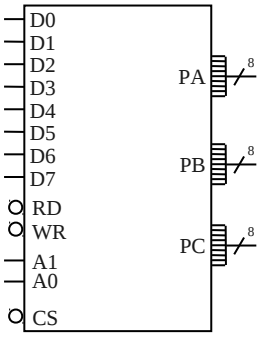
8253
Programmable Timer



74LS138
3-to-8 Line Decoder



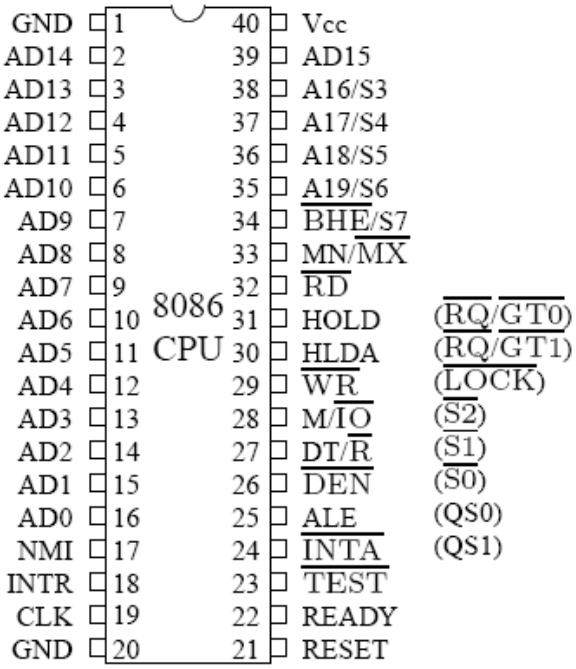
74LS245
Bus Transceiver



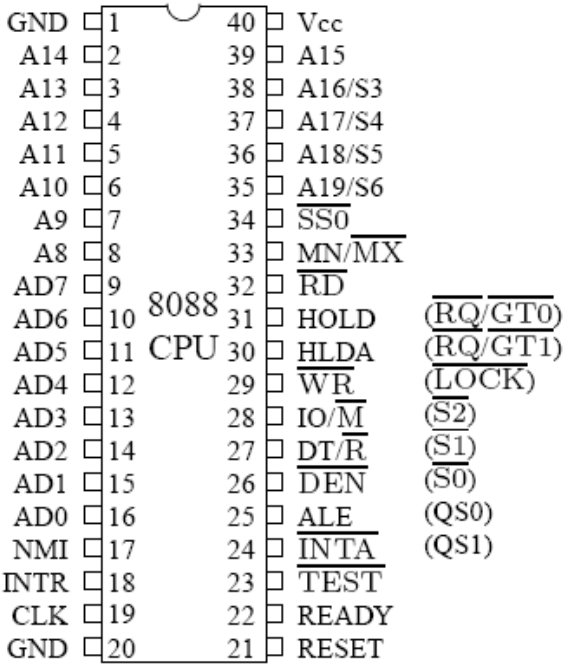
82C55 Programmable
Peripheral Interface

Standard Logic Gates: AND, NAND, NOT, OR, NOR, …

Intel 8086



Intel 8088



Max mode shown in (brackets)