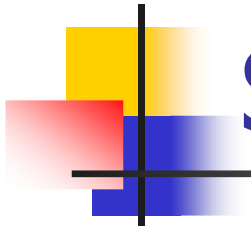
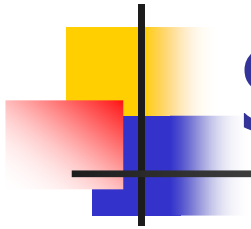
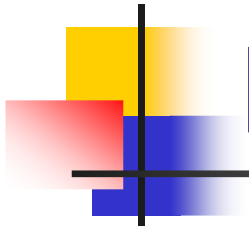


SYSC 3006 Review



SYSC 3006 Review

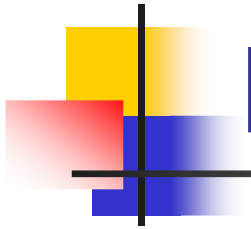
- Title: Computer Organization
  - Information Encoding : Signed/Unsigned/ASCII/instructions
  - CPU Programmer's Model: Registers, Instructions, Addressing Modes, Sequential Execution Model
  - Programming Constructs in Assembly: Arrays, Structures, Subroutines, Traps
  - I/O Programming
  - (Hardware) Interrupt Execution Model



Part I

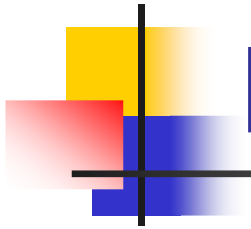
- Concrete components of a computer architecture (80x86):
  - registers, instructions, addressing modes,
  - memory organization,
  - I/O organization

- Programming this architecture in Assembly (Assembly Language is a TOOL for understanding concepts)



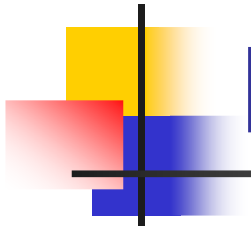
Part II

- I/O Devices functionality on IBM PC
- Know how to program access to these devices
- NO MEMORIZING. Know concepts and behaviours of I/O devices. Know how to :
  - (1) Read Port descriptions and be able to set **bitmasks**
  - (2) Program **sequence** of required operations



Part III

- Interrupt Processing Sequence
- Interrupt Programming (1) Install vector (2) Program ISR and (3) enable interrupts
- ISR Programming: No waiting loops! All information is maintained in global variables
- Event-driven mindset : Synchronization of fore/background threads, critical sections



Final Exam

- 3 hour, closed book, no aids (i.e. calculators)
- Kinds of questions
  - Concepts: Describe in words…
    - Define, Compare, Analyze …
  - Programming: Solving problems in assembly
    - Small cheat sheet of instructions provided on back page
  - Design: Solve a high-level problem, parts in assembly and/or pseudo-code

Content: **ALL COURSE MATERIALS**

- several copies of previous exams in IEEE Student Office and EngSoc Exam Library