**CARLETON UNIVERSITY**
**Department of Systems and Computer Engineering**
**SYSC 3601 Microprocessor Systems Summer 2007**
# Course Handout

## *Lecturer:*

**Professor Jim Green**, Room 4488ME, e-mail jrgreen@sce.carleton.ca (Please include "SYSC3601" in the subject line to ensure a response)

**Office hours**: 1st hour of each lab session in 4135ME or by appointment. See course web site for additional hours.

## *Course Objectives:*

To familiarize students with microprocessor-based circuit design. The course deals with the applications, organization, architecture, and design of microprocessor systems. Topics covered include addressing, bus structures, memory and I/O interfacing, interrupt mechanisms, and related techniques at the hardware and assembly language levels.

## *Prerequisites:*

ELEC2607 and SYSC2003 or Permission of the Department (request permission using the online form at www.sce.carleton.ca/ughelp). Students must satisfy the prerequisites in order to remain registered in the course. Students who have not completed the prerequisites are required to **withdraw** from the course or they may be deregistered from the course after the last day for course registration.

## *Textbook:*

Barry B. Brey, *"The Intel Microprocessors: 8086/8088, 80186, 80286, 80386, 80486, Pentium, Pentium Pro Processor, Pentium II, Pentium III, Pentium 4 Architecture, Programming, and Interfacing,"* Fourth, Fifth, Sixth, or Seventh Edition, Prentice Hall, QA76.8.12674B75, 1997, 2000, 2003, 2006. Note that a copy will also be made available for loan in the IEEE office.

## *Web Page:*

The course web page can be located at www.sce.carleton.ca/courses/sysc-3601/. Students are required to check this page often for course updates. Supplementary lecture notes will be posted there for student use. Note that reading the supplementary lecture notes only is **NOT ENOUGH** to pass this course! The single best predictor of student performance is attendance at lectures and labs.

## *Other References:*

- J.L Antonakos, *"The 68000 Microprocessor,"* Prentice Hall, QA76.8.M6895A57, ISBN 0-13-668120-4.
- Vranesic and Zaky, *"Microcomputer Structures,"* Holt, Rinehart & Winston, QA76.5.V73, 1989.
- Singh, W. Triebel, *"16-bit and 32-bit Microprocessors: Architecture, Software, and Interfacing Techniques, "* Prentice Hall, QA76.5.A93, 1991.
- 8086/8088 User's Manual Programmer's & Hardware Reference Guide, Intel. (Available in lab)
- SDK-86, MCS-86 System Design Kit User's Guide, Intel. (Available in lab).
- SDK-86, MCS-86 System Design Kit Monitor Listing (Available in Lab).
- Microprocessors Handbook, Intel 1990. (Available in Lab)
- Peripherals Handbook, Intel 1990. (Available in Lab).
- Additional materials may be made available on the course website.

## *Grading Scheme:*

- 10% Laboratory (Note that peer assessment may be included)
- 5% Term Assignment
- 12.5% Mid-Term Exam 1 (In-class, Closed Book, No Calculators)
- 12.5% Mid-Term Exam 2 (In-class, Closed Book, No Calculators)
- 60% Final Examination (Scheduled, 3 hours, Closed Book, No Calculators).

## *Important Notes:*

1) **Students must pass the Final Examination Paper** (50% or higher) in order to pass the course. (i.e. Failing to pass the Final Examination results in an F grade for the course). The final examination is for evaluation purposes only and will not be returned to the students.

2) **Students are expected to attend all lectures and labs.** If a student is absent from a lecture, it is up to the student to obtain missed lecture material from colleagues in the course. Attendance will be taken in the labs. Students will be given one, and only one, opportunity to make up a missed lab (and only one lab can be made up at an alternate time). Students who fail to submit any single lab report (out of the 5 labs) will receive a grade of zero for that lab. **Students who fail to submit two or more lab reports will be assigned a grade of zero for the entire lab component of the course (i.e. 0/10).**

3) **Students who miss the midterm** due to illness must provide a valid medical certificate to the instructor not later than 48Hrs after returning to campus. The certificate must clearly state the name of the doctor with contact information. Once the certificate has been verified, the midterm weight will be added to the final examination weight (i.e. the final exam becomes worth 85% of your final mark).

4) **Students with disabilities** requiring academic accommodations in this course are encouraged to contact a coordinator at the Paul Menton Centre for Students with Disabilities to complete the necessary letters of accommodation. After registering with the PMC, make an appointment to meet and discuss yours needs with me at least two weeks prior to the first in-class test or CUTV midterm exam. This is necessary in order to ensure sufficient time to make the necessary arrangements. Please note the following deadlines for submitting completed forms to the Paul Menton Centre: June 8th, 2007 for the Spring Term.

5) **Plagiarism** (e.g. copying and handing in for credit someone else's work) is a serious instructional offence that will not be tolerated. Please refer to the section on instructional offences in the Undergraduate Calendar for additional information.

6) **Deferred Exams.** Students who miss the final exam may be granted permission to write a deferred examination (see the Undergraduate Calendar for regulations on deferred exams). These students have additional months to study and a less crowded examination schedule compared to their colleagues who write the final exam in June. As such, it is only fair to expect substantially better performance from these students on the deferred examination than on the June final exam.

7) **Electronics Students** are required to take ELEC 4601, not SYSC 3601, in order to complete their program. Only those electronics students who have obtained special permission from both the Department of Electronics and the Department of Systems and Computer Engineering will be allowed to remain registered in SYSC3601.

8) Please note that there are **no lab exemptions** from this course, even for those repeating the course.

9) *Satisfactory performance during the term* includes attending all labs, and submitting and passing all labs, the assignment and the midterm. Attendance at lectures is also mandatory and fully expected.

## *Health and Safety:*

Every student should have a copy of our Health and Safety Manual. An electronic version of the manual can be found at:

http://www.sce.carleton.ca/courses/health-and-safety.pdf

## *Breakdown of Topics Covered (order subject to change)*

| | |
|---|---|
| 1. **Background and Introduction**<br>• Microprocessor history, types, applications and selection<br>• General microprocessor architecture<br>• Review of number systems<br>• Intel and Motorola microprocessor families | 2. **The Intel 80X86/88 Architectures and Programming**<br>• Registers and Internal Architecture<br>• Address generation and addressing modes<br>• Instruction set and assembly language programming<br>• The SDK-86 System Development Kit |
| 3. **The Intel 80X86/88 Bus and Buffering**<br>• 80X86/88 Pin functions, states, bus cycles and signalling waveforms<br>• Clock generators (Intel 8284) & bus controllers (Intel 8288)<br>• Latches (74373) & bus transceivers (74245)<br>• Wait states and bus timing | 4. **Memory Structures and Interfacing**<br>• Memory types and characteristics (DRAMs, SRAMs, ROMs, EPROMs, … )<br>• Address decoding<br>• Memory interfacing |
| 5. **Input/Output Systems (I/O)**<br>• Programmed I/O structures<br>• I/O ports design and address decoding<br>• Programmable Peripheral Interface Chips (Intel 8255A)<br>• Keyboard/Display Interface (8279) | 6. **Interrupt Systems**<br>• Interrupt Types (HW, SW & Exceptions)<br>• Interrupt structures<br>• Programmable Interrupt Controllers (Intel 8259 PIC)<br>• Programmable Counters/Timers (8253) |
| 7. **Direct Memory Access**<br>• Introduction to DMA structures<br>• Intel 8237 DMA Controller | 8. **Motorola 680X0 Microprocessor Architecture**<br>• Basic architecture and register structure<br>• Address generation and addressing modes<br>• Assembly language programming |
| 9. **Motorola Memory and I/O Structures**<br>• Memory organization and interfacing<br>• I/O interfacing<br>• Interrupt and exception vectors and INTA Cycle<br>• Vectored and autovectored interrupts | 10. **Floating Point Coprocessors**<br>• Co-processor architecture (Motorola or Intel)<br>• Coprocessor programming and interfacing |
| 11. **Serial Communications & Other Interfacing Chips**<br>• Synchronous vs. asynchronous communications<br>• Programmable communication interfaces (Intel 8251A USART) | 12. **Other Microprocessors and Bus Structures**<br>• Intel Pentium and Pentium Pro microprocessors<br>• Motorola 68020, 68030, 68040, and 68060 microprocessors<br>• Motorola 68HC11 Microcontroller family<br>• System buses (ISA, PCI, VME, … ) |
| 13. **Miscellaneous Topics and Review**<br>Possible topics include:<br>• Microcontrollers<br>• RISC vs. CISC architectures<br>• Introduction to DSPs | |